Antti Myllynen

Laterally doped III-V diodes for large-area optoelectronics

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Thesis supervisor:

Prof. Sami Franssila

Thesis advisor:

D.Sc. Jani Oksanen

Aalto University
School of Chemical Technology

AALTO UNIVERSITY
SCHOOL OF CHEMICAL TECHNOLOGY

ABSTRACT OF THE
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Advisor: D.Sc. Jani Oksanen

Conventional light-emitting diode (LED) designs experience current crowding and efficiency droop that limit their use in high-power applications. These problems could be solved with a recently proposed diffusion-driven current transport (DDCT) concept, that utilizes electron and hole diffusion currents as an injection method. So far, DDCT devices with lateral heterojunctions (LHJ) have been realized with selective-area growth (SAG) and ion implantation of GaN. However, these methods are quite challenging, complicated and expensive. Selective diffusion doping studied in this work could provide a simpler and more cost-effective fabrication technique for realizing lateral DDCT devices based on conventional III-V compound semiconductors.

This thesis investigated the performance of laterally doped GaAs/AlGaAs double heterojunction (DHJ) LEDs by simulations, and the selective-area diffusion doping methods needed to realize such devices in practice. First simulations of the LEDs studied the fundamental properties, requirements and limitations of the devices. Diffusion doping of n-type GaAs and GaAs/AlGaAs DHJ substrates from a Zn thin film dopant source, protected by a spin-on glass (SOG) film, was experimentally studied. Additionally, the viability of the developed doping method for realizing the DDCT devices was evaluated.

The simulations indicated that high-efficiency LEDs with an internal quantum efficiency of over 99.4 %, with highly uniform radiative recombination within the active region of the LED, can be achieved with high quality materials. Fabricated samples were characterized with current-voltage (IV) and light emission measurements, and visually inspected with a scanning electron microscope (SEM) and an optical profilometer. Vertical LEDs were successfully fabricated on both substrates, although some indications of substrate degradation was observed in the IV-characteristics of the devices.

Keywords: Light-emitting diode, Selective diffusion doping, Lateral heterojunction, LHJ, Diffusion-driven current transport, DDCT, III-V, SOG, Large-area, GaAs, AlGaAs, LED, DDCT, DILED

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Perinteiset hohtodiodirakenteet ovat alttiita virran ahtautumiselle sekä hyötysuhteen heikkenemiselle, mikä rajoittaa niiden käyttöä suurta tehoa vaativissa sovelluksissa. Mahdollisena ratkaisuna ongelmaan on hiljattain ehdotettu uutta virransyöttömenetelmää (DDCT engl. diffusion-driven current transport), joka käyttää elektronien ja aukkojen diffuusiovirtoja LEDin injektointimenetelmänä. Tähän mennessä DDCT:tä hyödyntävien lateraalisten GaN rakenteiden valmistamiseen on sovellettu selektiivistä epitaksiaa (SAG engl. selective-area growth) sekä ioni-istutusta. Nämä valmistustekniikat ovat kuitenkin hyvin haastavia, monimutkaisia ja kalliita. Diffuusioseostusmenetelmät voisivat tarjota yksinkertaisen ja kustannustehokkaan tekniikan DDCT laitteiden valmistamiseksi perinteisistä III-V yhdistepuolijohteista.

Tässä diplomityössä tutkitaan simulaatioiden avulla lateraalisesti seostettujen GaAs/AlGaAs tuplaheteroliitos-LEDien suorituskykyä, sekä kokeellisesti selektiivisiä diffuusioseostusmenetelmiä, joilla simuloitujen laitteiden valmistaminen voisi olla mahdollista. Simulaatiot DDCT rakenteista selvittävät niiden perusominaisuuksia, vaatimuksia sekä rajoituksia. Kokeelliset tutkimukset keskittyvät n-tyyppisten GaAs ja GaAs/AlGaAs substraattien diffuusioseostamiseen sinkkiohutkalvoista, jotka suojattiin spin-on glass (SOG) kalvolla. Lisäksi arvioitiin seostusmenetelmien mahdollista käyttöä DDCT laitteiden valmistukseen.

Valmistetut näytteet karakterisoitiin virta-jännite- sekä valoemissio-mittauksilla, pyyhkäisyelektronimikroskoopilla sekä optisella korkeuskarkeusmittarilla. Vertikaalisia LEDejä valmistettiin onnistuneesti molemmille substraateille, mutta joitakin merkkejä substraatin laadun heikkenemisestä havaittiin esimerkiksi IV-mittauksissa. Simulaatiot osoittivat että rakennetta käyttäen voidaan toteuttaa LEDejä, joiden sisäinen kvanttihyötysuhde on yli 99.4 %, ja joiden säteilevän rekombinaation homogeenisuus aktiivisessa alueessa on korkea.

Avainsanat: Hohtodiodi, Puolijohdevalaistus, Diffuusio, Seostaminen, Diffuusioseostaminen, DDCT, DILED, LED, GaAs, AlGaAs, DHJ, Yhdistepuolijohteet, III-V, Lateraalinen heteroliitos, SOG

Preface

First, I want to thank Professor Sami Franssila for supervising my thesis. Great thanks also belong to D.Sc Jani Oksanen, my advisor, for his invaluable help and guidance during my thesis, and the possibility of working with such an interesting topic. Great thanks goes also to Toufik Sadi, who guided me through the device simulations, and whose simulation model was adapted to the use of this thesis. Also, big thanks to Ivan Radevici who helped me with the experiments, and Tuomas Haggren who fabricated the GaAs/AlGaAs samples and the reference p-n samples with MOVPE. I want to thank also Pyry Kivisaari and Alberto Casado for relaxing discussions, and the rest of our research group and other colleagues for all the support during my thesis.

I want to thank also my parents who have always supported me to reach my dreams. Finally, the greatest gratitude of all goes to Riikka, my fiancée, for all the support, patience and love.

Otaniemi, 12.04.2018

Antti I. Myllynen

Contents

Symbols and abbreviations

Symbols

A	Shockley-Read-Hall recombination coefficient
a	Lattice constant
B	Radiative recombination coefficient
b	Bowing parameter
C	Auger recombination coefficient
C_{Zn}	Zn concentration
D	Diffusion constant
D_0	Temperature-independent diffusivity
d	Thickness of the active region
dC/dx	Concentration gradient
E_A	Activation energy
E_a	Acceptor energy level
E_C	Conduction band energy
E_d	Donor energy level
E_F	Fermi level
E_{Fn}	Quasi-Fermi level for electrons
E_{Fp}	Quasi-Fermi level for holes
E_g	Band-gap energy
E_V	Valence band energy
ϵ	Permittivity
$F_{1/2}$	Fermi integral of the order 1/2
f_e	Fermi-Dirac distribution of electrons
h^+	Hole
I	Current
I_0	Reverse saturation current
I_{Ga}	Interstitial gallium atom
J_D	Diffusion flux
J	Current density
J_n	Current density for electrons
J_p	Current density for holes
j_s	Surface recombination rate
k	Boltzmann constant $\approx 1.381 \times 10^{-23}$ J/K
m	Ideality factor
n	Electron concentration
n_s	Carrier density at surface
N_A	Acceptor concentration
N_D	Donor concentration
n_i	Intrinsic concentration
p	Hole concentration
q	Elementary charge $\approx 1.602 \times 10^{-19}$ C

Q_{Zn}	Amount of deposited Zn (at/cm^2)
R	Total recombination rate
R_{aug}	Auger recombination rate
R_{rad}	Radiative recombination rate
R_{srh}	SRH recombination rate
S	Surface recombination velocity
T	Temperature
τ_n	SRH lifetime for electrons
τ_p	SRH lifetime for holes
μ_n	Mobility of electrons
μ_p	Mobility of holes
V	Bias voltage
V_D	Diffusion voltage
V_{Ga}	Gallium vacancy
V_{th}	Threshold voltage
x_j	Junction depth
Zn_i^+	Positively charged interstitial zinc atom
Zn_s^-	Negatively charged substitutional zinc atom
Φ	Electrostatic potential
Φ_{SB}	Schottky barrier height
Φ_M	Metal work function
χ_{SC}	Electron affinity of semiconductor

Abbreviations

AR	Active region
CB	Conduction band
CSL	Current-spreading layer
CVD	Chemical vapor deposition
DDCT	Diffusion-driven current transport
DHJ	Double heterojunction
DILED	Diffusion injected light-emitting diode
EB	Electron-beam
EDX	Energy dispersive x-ray spectroscopy
ELO	Epitaxial lift-off
FEM	Finite element method
FCC	Face-centered cubic
IV	Current-voltage
IQE	Internal quantum efficiency
LED	Light-emitting diode
LHJ	Lateral heterojunction
LPE	Liquid phase epitaxy
MBE	Molecular beam epitaxy

MOCVD	Metal-organic chemical vapor deposition
MOVPE	Metal-organic vapor phase epitaxy
MQW	Multi-quantum well
MS	Metal-semiconductor
PSG	Phosphosilicate glass
PVD	Physical vapor deposition
QW	Quantum well
RGB	Red-Green-Blue
RTA	Rapid thermal annealing
SAG	Selective-area growth
SEM	Scanning electron microscope
SIMS	Secondary ion mass spectroscopy
SOG	Spin-on glass
SRH	Shockley-Read-Hall
SSL	Solid-state lighting
VB	Valence band
VSI	Vertical scanning interferometry
YSZ	Yttria-stabilized cubic-zirconia
ZNO	Zinc nitrate

1 Introduction

At present, research topics related to energy consumption and production play a crucial role in answering the threat caused by the climate change. Accordingly, the European Commission [1] has set several targets for the climate and energy strategies. By the year 2030, these targets include for example a 40 % reduction in greenhouse gas emissions from the 1990 level and a 27 % renewable energy contribution to the total energy production. Additionally, according to the 2012 Energy Efficiency Directive [2], at least a 27 % improvement in energy efficiency throughout the whole energy chain, from production to final consumption should be achieved. Reaching these goals requires advances on several technological fields including photonics and optoelectronics.

Solid-state lighting (SSL), especially light-emitting diodes (LED), have already revolutionized the lighting industry, but the field is still developing quickly. Since the realization of the first high-efficiency blue LED in 1994 [3] enabling the production of white LEDs, SSL has started replacing incandescent lamps. This development is still ongoing in industrial as well as domestic applications with ever increasing power and cost requirements. The increased use of LEDs has lead to decreased energy consumption of lighting systems, and for example in the US, it has been estimated that this would result in energy savings of 15 % in 2020 and 40 % in 2030 if compared to year 2013. This development would mean annual savings of over $26 billion in the year 2030 with current prices in the US alone [4].

Beside blue LEDs, the interest on red and infrared LEDs based on III-V materials is expected to grow substantially due to their importance in several applications including automotive and traffic lights, red-green-blue (RGB) back-light systems, green house plant illumination [5] and potential new emerging fields such as thermophotonics [6]. However, the development of III-V based LEDs has been nearly dormant for the past decades, if compared to the development of GaN based LEDs. Consequently, the efficiency of III-V LEDs still lags behind the high efficiency blue LEDs [7], and is far from the theoretically achievable limits. Lately developed new fabrication methods such as epitaxial-lift off (ELO) [8, 9] have been recently used to realize the current state-of-the-art III-V LED based on InGaAlP [10]. Consequently, the effort put into developing III-V materials is increasing yet again.

This work studies the possibility of introducing a paradigm shift in the design of LEDs by fundamentally changing both the current injection principle and the device structure. Fig. 1(a) illustrates a conventional flip-chip design where the active region (AR) is sandwiched between a p- and n-type barrier regions and whose efficiency is in part limited by current crowding, resistive losses and the required etching through the AR. Fig. 1(b) presents the studied new GaAs/AlGaAs double heterojunction (DHJ) LED that is also simulated for the first time in this work. This structure utilizes lateral heterojunctions (LHJ) and a recently proposed diffusion-driven current transport (DDCT) method [11, 12, 13, 14] that exploits bipolar diffusion of charge carriers to inject them into the active region of the LED.

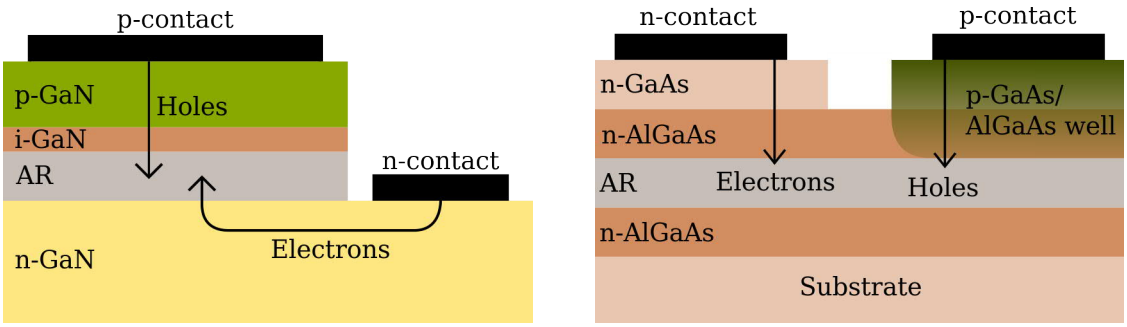


Figure 1: (a) Conventional flip-chip LED designs suffer from several issues such as current crowding and resistive losses. (b) Novel GaAs/AlGaAs based DHJ LED structure utilizing the recently proposed DDCT current injection method to excite the active region.

In contrast to conventional DHJ LEDs, using DDCT enables unconventional device designs where the active region is located outside of the p-n junction. This kind of structure allows the injection of electrons and holes from the same side of the AR, meaning that etching through the active region can be avoided, and the lateral transport distances in the device can be minimized. This is important for LEDs with thin current spreading layers, fabricated on insulating substrates such as GaN or sapphire, or in thin-film devices separated from the substrate. This should help to avoid the above-mentioned problems of flip-chip LEDs [15, 16]. Additionally, by removing the substrate entirely, DDCT should enable structures with near surface active regions, that could then be further processed, for example, to increase the light extraction with surface plasmons [17]. In the future, DDCT LEDs and devices could also be used to realize efficient solar cells or to improve charge spreading in more demanding applications such as thermophotonic heat pumps [18] or double diode structures [19, 20, 21] studying electroluminescent cooling.

Realizing the device presented in Fig. 1(b) requires lateral doping of the structures by unconventional fabrication processes such as diffusion doping or ion implantation that have not typically been used for LED fabrication despite the fact that their potential use has been previously discussed in the context of laterally injected lasers [22, 23, 24]. Such methods have also been studied in the early days of the LED industry, but they have been nearly superseded by in-situ doping during the epitaxial growth of the device layers. First DDCT structures were very recently demonstrated with selective-area growth (SAG) [15, 16] and selective-area ion implantation [25]. However, especially for GaAs based devices, it would be much more convenient to be able to replace these techniques by selective-area doping processes to fabricate the p-doped region of the lateral p-n junction. One of such processes for GaAs is Zn diffusion doping that has been extensively studied in 1970-1990, after which its popularity has declined due to diminished need for post-growth doping processes. Recently, zinc doping of n-type GaAs substrates from Zn doped spin-on-glass (SOG) films was investigated in our group, but the obtained Zn concentrations were not yet sufficiently high to fabricate p-n junctions [26].

The goal of this thesis is to evaluate the general requirements and limits of the proposed DDCT structure by simulations, and to experimentally study if the selective Zn diffusion doping method employing other dopant sources could be used to fabricate the structure. Based on the simulations, the proposed DDCT structures can be highly efficient. Additionally, the fabrication of vertical LEDs have been successfully demonstrated with diffusion doping.

This thesis reviews the fundamental properties of semiconductors as well as the simulations and experiments carried out by the author, and is organized as follows: Section 2 explains the fundamental properties of semiconductor materials including a brief introduction into III-V semiconductors, more detailed review about doping mechanisms and different doping processes, and finally a brief overview about lateral device doping. In Section 3, basic aspects of LED physics, most important recombination processes, LED structures and electrical contacts are reviewed. Section 4 briefly introduces the computational model used in the simulations. Materials and methods used in the experimental studies are presented in Section 5. Finally, results and discussion are provided in Section 6, followed by the conclusions in Section 7.

2 Fundamental properties of semiconductors

This Section starts by a brief introduction to semiconductor materials and their fundamental properties to provide the general framework for this work. Next, III-V compound semiconductors including GaAs and AlGaAs are discussed and a short overview of their thermal stability is given to introduce the challenges associated with the hight temperatures often encountered during device fabrication. Then, different doping methods based on both diffusion and ion implantation processes for doping of GaAs and AlGaAs are reviewed. Finally, lateral device fabrication methods such as selective doping and selective-area growth are discussed.

2.1 Introduction to semiconductor materials

Semiconductor materials such as silicon and gallium arsenide used in high-performance devices are typically single crystalline materials. Generally, crystalline materials are formed when individual atoms are covalently bonded to each other and a periodic atomic lattice is formed. Before the physically stable lattice is formed, the system can be thought to consist of individual atoms with relatively large separation distance and discrete energy levels. Fig. 2 illustrates that as the separation is reduced and atoms start to bond together, the energy levels begin overlapping and splitting into a series of closely spaced electron states. As the number of atoms and thus electrons

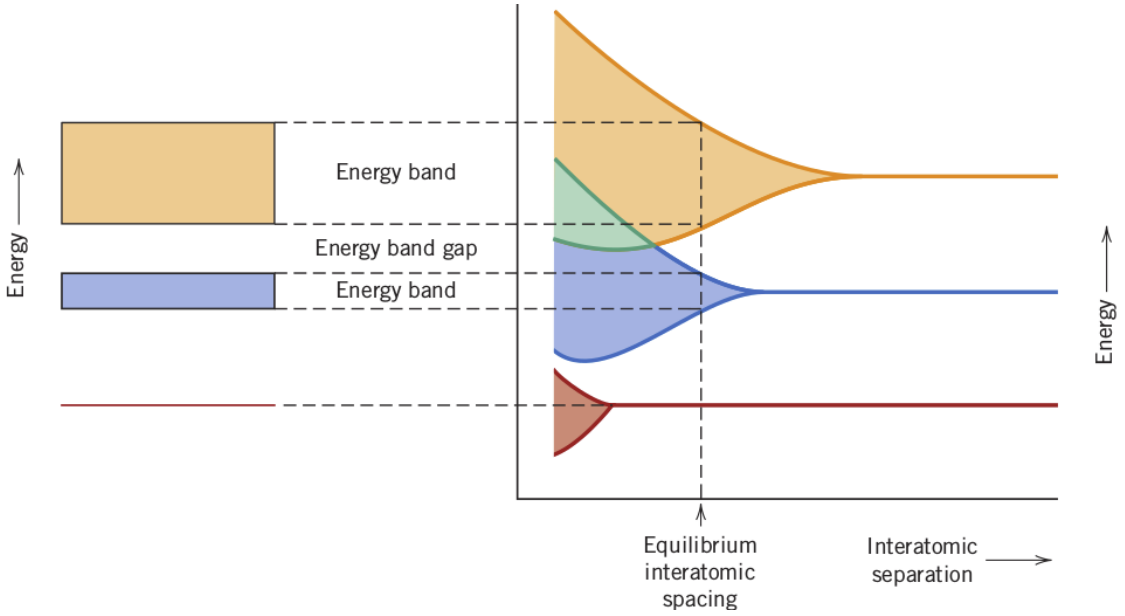


Figure 2: A typical representation of the formation of the energy bands of a solid material in equilibrium. On the right, electron energy levels are shown as a function of interatomic separation. Bands are formed when the separation reduces towards the equilibrium interatomic spacing. The left section of the image highlights how the typical energy bands of a solid material are distributed over energy (y-axis) and space (x-axis) when the atomic separation corresponds to the equilibrium value [27].

in the lattice increase and the distance between adjacent electron states become exceedingly small, the closely spaced states will form several quasi-continuous energy bands. These bands can be either partially filled or empty. In addition, some energies might be forbidden, so band-gaps can also exist in the energy band diagram. [27]

The electrical properties of solid materials are defined by their electronic band structure and Fermi energy level E_F, which corresponds to the energy of the highest completely filled state at temperature of 0 K. Generally, all electrons having energy within a few kT around the Fermi level can participate in the conduction process. In conductors, the Fermi level is within a partially filled energy band, so that a large number of electrons can participate in the electrical conductance. In semiconductors and insulators, the Fermi level is within a band-gap where electron states do not exist in a perfect crystal. For insulators, the band-gap energy is so high that only few thermally excited electrons can be promoted across the band-gap to conduct electricity. For semiconductors, the band-gap energy is smaller, meaning that more electrons will have enough energy to be excited across the band-gap to the conduction band (CB). Additionally, electron vacancies called holes in the top of the valence band (VB) can contribute to charge transport in semiconductors. [27]

Band-gaps are classified as direct and indirect, based on the relative position of the valence band maxima and conduction band minima. In direct band-gaps, the valence band maxima and the conduction band minima are located at the same k-vector value in the reciprocal space, which enables radiative electron-hole recombination resulting in photon emission as light. In indirect band-gaps, the conduction band minimum and valence band maximum do not line up, meaning that electrons and holes can only recombine with non-radiative or phonon-assisted second order processes. [28]

The most important reason for the technological importance of semiconductors is that their electrical properties and behaviour can be further adjusted with a doping process by adding impurity atoms into the lattice structure. These dopant atoms can introduce additional electrons to the conduction band of the material or generate holes into the valence band. A more detailed overview of doping is given in Subsection 2.3.

Several semiconductors are used in multiple application areas but silicon is by far the most common semiconductor material which has revolutionized the microelectronics industry. Silicon is an excellent material for electronics because it is abundant and relatively cheap, and the fabrication processes for Si based devices are also extremely well matured. However, silicon has an indirect band-gap which makes it a very poor material for light emitting devices such as lasers and LEDs, and less than ideal also for light absorbing devices such as solar cells. This shortage is answered by devices based on III-V semiconductor materials such as GaAs, AlGaAs, GaN and InP.

2.2 III-V semiconductors

III-V compound semiconductors are very important materials for modern optoelectronic devices due to a high number of direct band-gap materials within the group. Typical applications for these semiconductors are high performance LEDs, lasers and solar cells [29, 30]. Conventional III-V compound semiconductors are alloys of group

III elements (Al, Ga, In) and group V elements (As, N, P, Sb). These elements can form several alloys but generally binary, ternary and quaternary compounds that consist of two, three and four elements respectively are used.

Fig. 3 shows the band-gap energy E_g as a function of lattice constant a for typical III-V compound semiconductors. All binary compounds such as GaAs and AlAs are marked as single points, since they have only one composition and thus a single well defined value for both E_g and a. The band-gap energy and lattice constant of ternary systems depend on the composition of the alloys. The range of E_g and a values for these systems are indicated by the lines combining binary compounds. Furthermore, the areas delimited by these lines define the possible band-gap energies and lattice constants for quaternary systems.

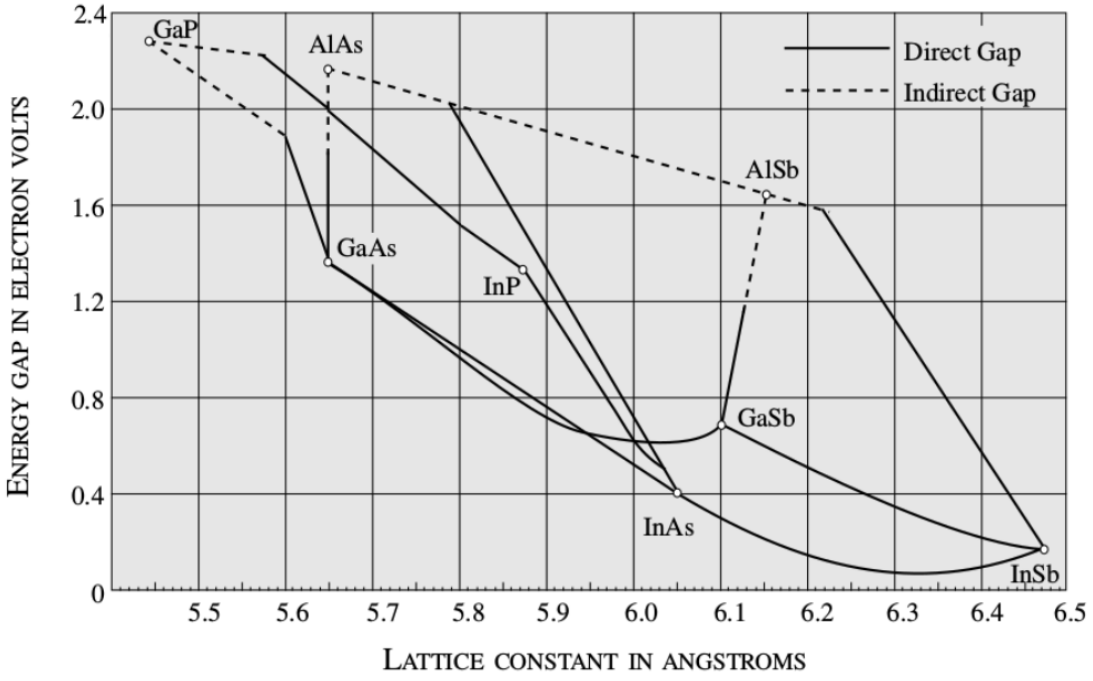


Figure 3: The lattice constants, band-gap energies and band-gap types of the conventional III-V semiconductors. [31].

One of the advantages of ternary and quaternary compound semiconductors is that band-gap engineering can be used to tune the E_g by changing the composition of the alloy. However, it should be noted that simultaneously the lattice constant of the compound also changes. This limits the amount of feasible material combinations and compositions, since in epitaxial growth the lattice constant should stay roughly the same to avoid excess stress when layers are grown on top of each other.

Generally, the band-gap energy of ternary systems consisting of binary compounds AC and BC can be estimated with

$$E_g(A_{1-x}B_xC) = (1-x)E_g(AC) + xE_g(BC) - x(1-x)b, \tag{1}$$

where $E_g(AC)$ and $E_g(BC)$ are the band-gap energies for binary alloys AC and BC, and x is the molar fraction of BC material in the alloy. The so-called bowing parameter b describes the deviation from a linear interpolation between the two binaries. The sign of b is typically positive for III-V alloys, meaning that the actual band-gap energy is smaller than a linear interpolation would indicate. [30]

Band-gap engineering is an important tool for ternary and quaternary compound semiconductors since E_g determines the energy of the generated photons and thus the wavelength of the emitted light. Additionally, the type of band-gap for some materials such as AlGaSb and AlGaAs, can switch between direct and indirect depending on the stoichiometric composition of the alloy. [28]

Nowadays, a single III-V semiconductor material is rarely used in optoelectronic devices other than photovoltaics. Typically, several different compound semiconductors are used together to form heterojunctions, double heterojunctions or more complex material stacks. In a typical DHJ structure, a semiconductor material with a lower band-gap energy is placed between different semiconductor materials having a higher band-gap energy. The middle layer functions as an active layer of the device, where electrons and holes are confined due to the potential barriers that are created around it. The GaAs/AlGaAs material system used in this work is one suitable option for DHJ structures.

2.2.1 Gallium arsenide

The interest in gallium arsenide has been driven by its superior electronic transport properties, high electron mobility and suitable band structure for optoelectronic applications [32]. Additionally, the band-gap of GaAs is almost optimal for maximum possible theoretical conversion efficiency in single junction solar cells [33]. Due to the excellent properties of GaAs, it has become one of the most important and studied compound semiconductors. Already in the year 2005, GaAs market size was several billion dollars, though this was only a couple of percent of the whole microelectronics market which is mostly dominated by silicon [32].

GaAs is a binary compound with a zinc-blende crystal structure which has a face-centered cubic (FCC) translational symmetry [34]. Fig. 4 illustrates the unit cell of GaAs. The zinc-blende structure consists of two inter-penetrating FCC lattices, one consisting of gallium and the other of arsenic [30]. The structure has a tetrahedral coordination, meaning that each atom forms four bonds with the closest neighboring atoms of opposite type.

GaAs can be produced as wafers by several methods including Czochralski and Bridgman techniques. Both methods utilize a seed crystal with a desired orientation and a GaAs melt that crystallizes in the same orientation as the seed crystal. GaAs wafers can be used as substrates, on top of which devices can be fabricated. Other production methods for GaAs are epitaxial growth techniques including liquid phase epitaxy (LPE), metal-organic vapor phase epitaxy (MOVPE) and molecular beam epitaxy (MBE). These methods are used to produce thin films of single-crystalline GaAs on a substrate. [32]

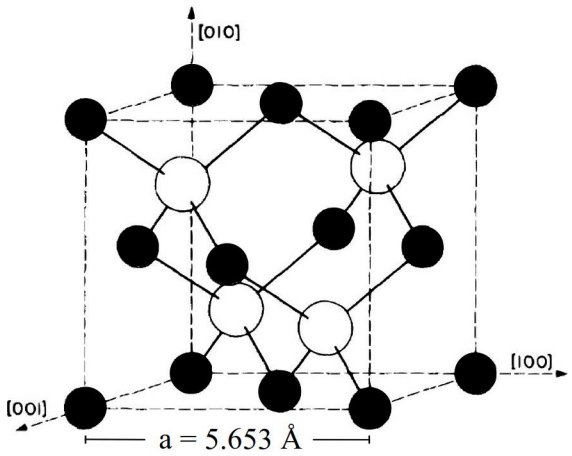


Figure 4: Unit cell of GaAs where black spheres represent gallium atoms and white spheres represent arsenic atoms. Each Ga atom is bonded to four As atoms and each As atom is bonded to four Ga atoms. The distance between neighboring atoms is 2.448 Å. [34].

One important property of GaAs is its direct band-gap at the Γ-point with a band-gap energy of 1.42 eV. This enables efficient inter-band recombination of electrons and holes in which photons are emitted. Fig. 5 represents the electron band structure of GaAs.

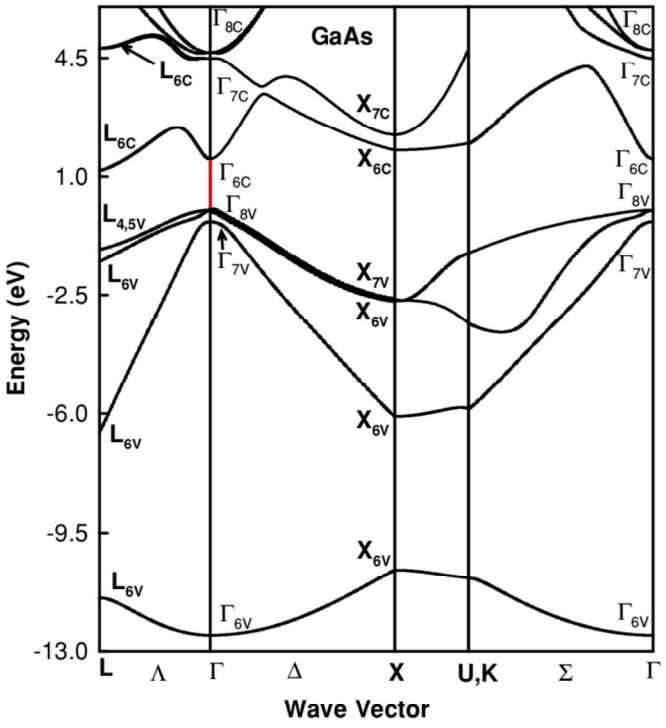


Figure 5: The electronic band structure of GaAs. The direct band-gap at the Γ-point is highlighted in red. The conduction and valence bands are marked with subscripts C and V, respectively. [35]

Additionally, GaAs has a very high electron mobility which is the result of a small electron effective mass in the material. Fig. 6 shows that the electron drift velocity in GaAs is generally higher compared to other materials at low electric field strengths. However, as the electric field increases above 10^4 V/cm the situation changes and the electron mobilitity of both InP and Si outperforms that of GaAs. [31] It should also be noted that the hole mobility in GaAs is significantly lower, representing only 5 % of the electron mobility [27]. This leads to slower p-type channel devices [36] and sets some additional limitations that limits the benefit of high electron mobility.

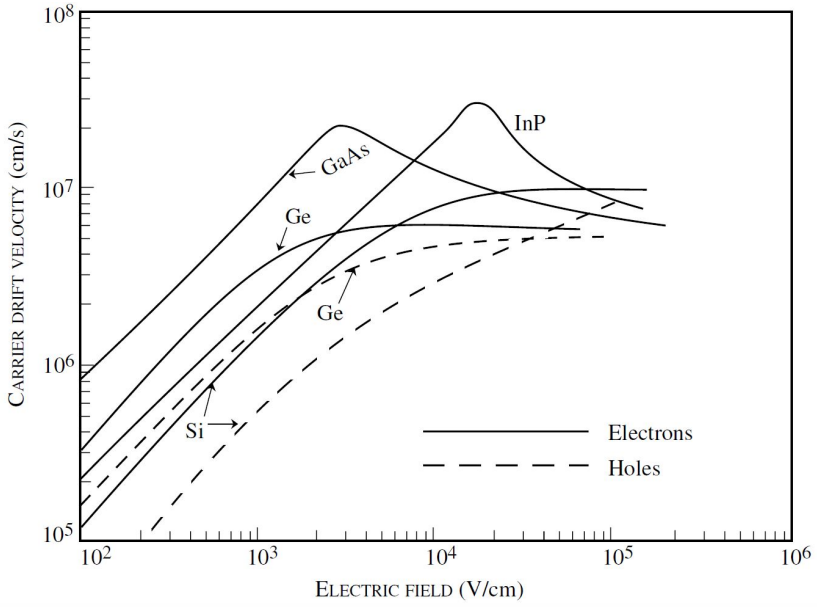


Figure 6: Carrier drift velocities for GaAs, Si, Ge and InP at different electric field strengths, showing that the highest drift velocities at field strengths below $\sim 10^4$ V/cm are achieved with GaAs. [31]

2.2.2 Aluminum gallium arsenide

Aluminum gallium arsenide a disordered alloy that is perhaps the most important ternary compound semiconductor for GaAs based devices. $Al_xGa_{1-x}As$ consists of GaAs and AlAs binary alloys, and has a zinc-blende structure. In addition, the lattice constant of AlGaAs is well matched to GaAs as can be seen in Fig. 3. The lattice constant a increases with aluminum composition and the exact value can be estimated with

$$a = 5.6533 + 0.0078x, \tag{2}$$

where x is the fraction of aluminum in the alloy. This means that multi-layered $GaAs/Al_xGa_{1-x}As$ structures with a thickness of several 100s of nm can be grown on top of GaAs substrates without excessive strain energy build-up. [31, 37, 38]

Generally, the band-gap energy of ternary and quaternary compound semiconductors depends on the alloy composition and can be calculated with simple equations. For $Al_xGa_{1-x}As$, direct band-gap energy for $0 \leqslant x \leqslant 0.45$ can be calculated with

$$E_g^{\Gamma}(x) = 1.424 + 1.247x, \tag{3}$$

and indirect band-gap energies for $0.45 \leqslant x \leqslant 1.0$ can be calculated using

$$E_g^{L}(x) = 1.708 + 0.642x \tag{4}$$

and

$$E_g^{X}(x) = 1.900 + 0.125x + 0.143x^2. \tag{5}$$

As seen from Eq. (3) – Eq. (5), other important aspect of AlGaAs compounds is that their band-gap switches from direct gap to indirect as the mole fraction of aluminum increases above 45 % in the alloy [31, 37]. Fig. 7 represents the band diagrams for $Al_xGa_{1-x}As$, with selected Al-compositions x.

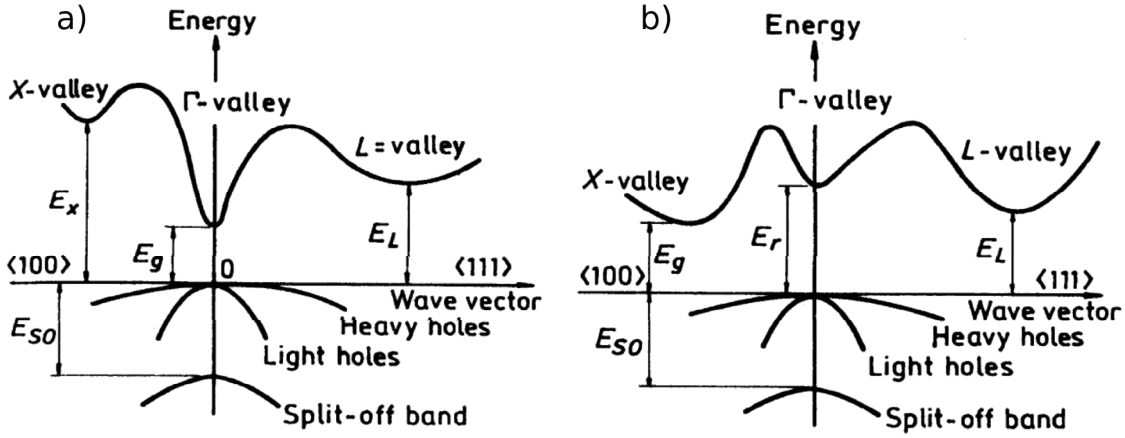


Figure 7: Band diagrams for $Al_xGa_{1-x}As$. (a) Illustration of direct band for $x < 0.45$. (b) Representation of indirect band-gap for $x > 0.45$. The exact energies of Γ, X and L valleys depends on the composition of $Al_xGa_{1-x}As$. [39]

Excellent lattice matching to GaAs, adjustable band-gap energy and the transition between direct to indirect band-gap are important properties of $Al_xGa_{1-x}As$ that enable the fabrication of semiconductor devices based on GaAs/AlGaAs heterojunctions or double heterojunctions. DHJ structures utilize larger band-gap of $Al_xGa_{1-x}As$ to confine electrons and holes in the GaAs active layer, located between $Al_xGa_{1-x}As$ barrier layers. Additionally, photons that are emitted in the active layer are not re-absorbed into the $Al_xGa_{1-x}As$, as AlGaAs is a transparent material. Heterojunctions are used in several applications including optoelectronic devices such as lasers, LEDs and solar cells, and high-speed electronics. [37, 40] The use of $GaAs/Al_xGa_{1-x}As$ heterostructures is discussed more closely in Subsection 3.4.

2.2.3 High temperature stability of III-V semiconductors

Several microfabrication processes such as diffusion doping, damage annealing after ion implantation and contact annealing involve high temperatures. In the case of GaAs, AlGaAs and other III-V compound semiconductors, the use of elevated temperatures is generally problematic, due to the low thermal stability of these materials. Especially, group V element of the compounds is highly volatile at elevated temperatures which can lead to loss of stoichiometry at the specimen surface. Consequently, defects like vacancies and residual metallic bonds that can degrade the device performance can be formed. [41]

Haynes *et al.* [41] tested the evaporation rate of both Ga and As atoms from (100) oriented GaAs substrate with rapid thermal annealing system. Fig. 8 shows the evaporation rates of Ga and As atoms from substrate surface as a function of inverse temperature. Their results show that the evaporation rates of both Ga and As is in the range of 10^{13}–10^{14} atoms/cm^2 s at 600–650 °C. This means that protecting methods must be used if high temperatures are needed for device processing.

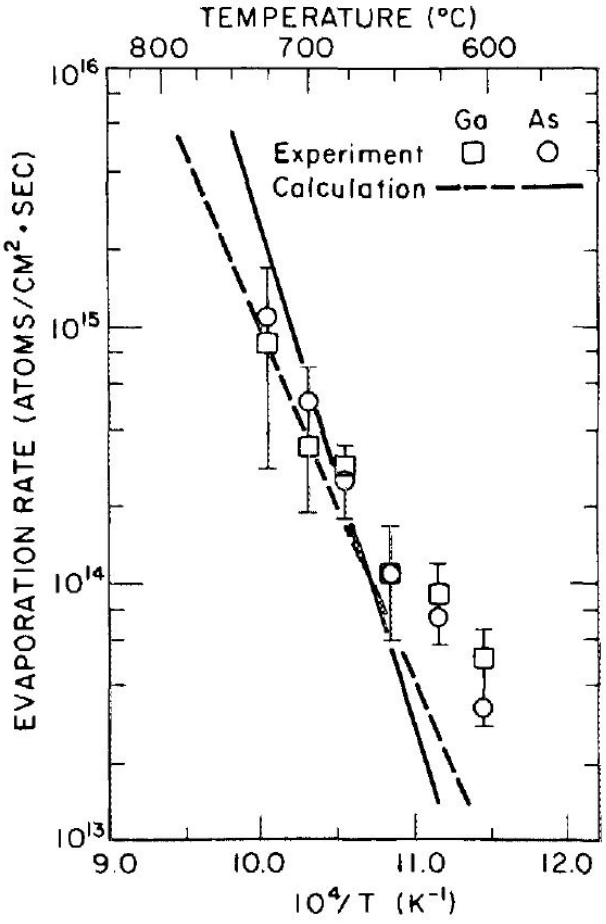


Figure 8: Evaporation rate of Ga and As from unprotected i-GaAs (100) wafer at the temperature range of 600–725 °C. Annealing was performed in a high-vacuum RTA system. [41]

Protection of GaAs substrates can be done with several methods or combinations of them. One effective technique is encapsulation of the samples with dielectric films such as spin-on-glass [42], phosphosilicate glass (PSG) [43, 44, 45], yttria-stabilized cubic-zirconia (YSZ) [46] or SiO_2 [43]. Alternatively, As or Ga overpressure or other protective atmospheres, including N_2 and Ar, can be used to suppress the out-gassing of the substrate [47, 48]. The role of annealing atmosphere is especially critical if no encapsulation is used, since the formation of GaAs surface oxides occurs readily if O_2 is present during the annealing leading to rapid desorption of the surface oxides [32]. Furthermore, RTA technique can be used to reduce annealing time which should reduces the extent of thermal degradation and simplify the necessary protection for the samples. [41] The use of these strategies can be clearly noticed in Subsections 2.3.3 and 2.3.4 where different doping methods are reviewed.

2.3 Doping of GaAs and AlGaAs

The main reason for the use of semiconductors is that their electrical properties and behavior can be altered by adding impurity atoms, called dopant atoms, into the crystal lattice of the materials. As was previously explained, only few electrons will have enough energy to move to the conduction band of the material, and practically no holes exist in undoped (intrinsic) materials. Dopant atoms introduce additional electrons or holes to the semiconductor material.

Fig. 9 illustrates common dopant and impurity atoms with the induced impurity energy levels in GaAs. Dopant atoms are either donors or acceptors depending on their interactions with conduction and valence bands. Donors have energy levels

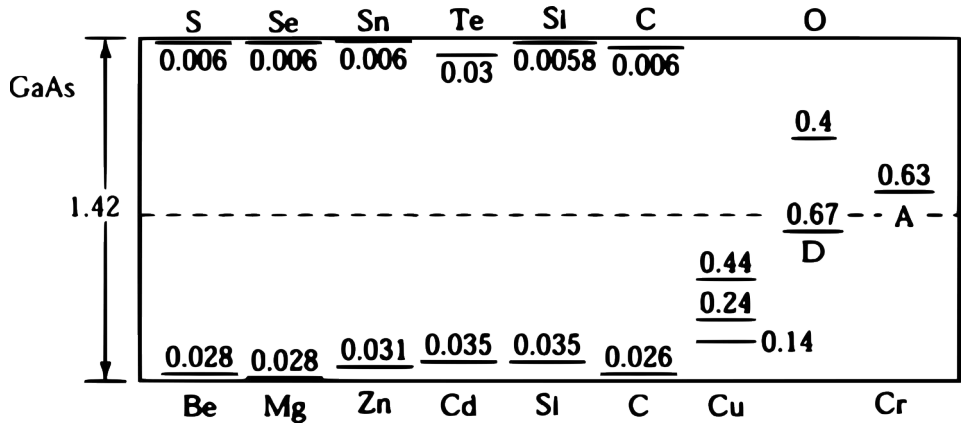


Figure 9: Common impurity atoms and their respective donor and acceptor energy levels measured from the corresponding band edge inside GaAs band-gap. The top of the image represents the conduction band edge, dashed line in the middle is the intrinsic Fermi level, and the bottom of the image represents the valence band edge. Atoms marked at the top and bottom of the Figure are donors and acceptors, respectively. Annotations A and D are clarifying that oxygen 0.67 energy level is predominantly a donor level and chromium 0.63 level is predominantly an acceptor level [49].

E_d typically slightly below conduction band, so they can release electrons into the conduction band with a small excitation energy that is easily available through thermal energy. Acceptors have energy levels E_a typically slightly above valence band so electrons from the valence band can easily jump into the acceptor levels. As electrons move to acceptor levels, holes are generated at the valence band. Donors are therefore used in n-doping (electrons as charge carrier) and acceptors in p-doping (holes as charge carriers). [36, 50]

Several dopant atoms exist for III-V semiconductors, but the most important dopant in the scope of this work is zinc, because it is the most suitable p-dopant for DDCT devices due to its high diffusivity and doping concentrations in both GaAs and AlGaAs. These properties enable relatively quick diffusion process which helps to avoid thermal decomposition of the substrates that was discussed in Subsection 2.2.3. When Zn atoms are located at Ga lattice sites they function as acceptors and create mobile holes to the valence band of GaAs. [51]

Other important dopant atoms for GaAs are group IV elements such as Si and Ge. Since these atoms have four valence electrons they can work as either n-dopant or p-dopant depending on the location of these atoms in the substrate lattice. Si and Ge are donors if they are at Ga lattice sites, since they have one additional valence electron compared to Ga. If they are located at As lattice site, the situation is reversed and they work as acceptors. This kind of dopant atoms are called amphoteric. [36, 52] In typical GaAs structures, Si preferentially behaves as a donor and is a commonly used dopant in GaAs substrates and epitaxy.

Typical n-type dopant atoms of group VI such as S, Se and Te are incorporated on the As lattice sites where they will function as donors. Selenium is a good dopant for ion implantation since it can only be at As sites and the achieved dopant concentration can be high. Tellurium is not suitable for ion implantation due to its relatively high mass, but it is good for heavily doped n-type epitaxially grown ternary layers. [36]

In addition to Zn, other p-dopant atoms are also available. Carbon is a very important shallow acceptor for doping during epitaxial growth due to its stability and the high concentration of over 10^{19} cm^{-3} that can be a achieved. However, it diffuses very slowly in GaAs. Beryllium is another important shallow acceptor that has a high electrical activity. Due to its slow diffusivity, Be-doping is generally carried out during epitaxial growth or by ion implantation. Magnesium is another dopant that has been used for III-V semiconductors. However, solid solubility and diffusivity of Mg in GaAs are lower when compared to Zn. [53].

Doping of semiconductors can be performed with several processes. Impurity atoms can be introduced into the material during crystal growth to dope whole ingots. Uniformly doped layers can be fabricated during epitaxial growth. Diffusion doping and ion implantation can be used for selective-area doping of the substrate surface regions. [54] To fabricate lateral DDCT devices, selective doping of the surface areas is needed, thus this thesis focuses on diffusion doping and ion implantation techniques.

2.3.1 Diffusion

Diffusion is the movement of atoms due to thermal motion along concentration gradients effectively from higher to lower concentration. Concentration-dependent diffusion flux can be described by Fick's first law

$$J_D = -D\frac{dC}{dx}, \tag{6}$$

where J_D is the flux in atoms/cm^{2}s, D is the diffusion constant in cm^2/s and dC/dx is the concentration gradient. The diffusion constant depends strongly on temperature which can be estimated with Arrhenius form

$$D = D_0 \exp\left(\frac{-E_A}{kT}\right), \tag{7}$$

where D_0 is a temperature-independent diffusivity in cm^2/s, E_A is the activation energy of the diffusion in eV, k is Boltzmann's constant in eV/K and T is the lattice temperature in K. In addition to temperature, the value of the diffusion coefficient is related to several factors, such as diffusion mechanism, crystal structure of the substrate and material quality including the number of defects and dislocations. [36, 54]

In general, three diffusion mechanisms exist. Fig. 10 illustrates the interstitial, substitutional and kick-out diffusion mechanisms. Also, combinations of these mechanisms are possible. Interstitial diffusion occurs via empty spaces between the lattice atom. The energy required for the diffusing atom to jump into neighboring interstitial sites increases as the size of the diffusing atom increases. Thus interstitial mechanisms are typical for smaller atoms. [36, 54]

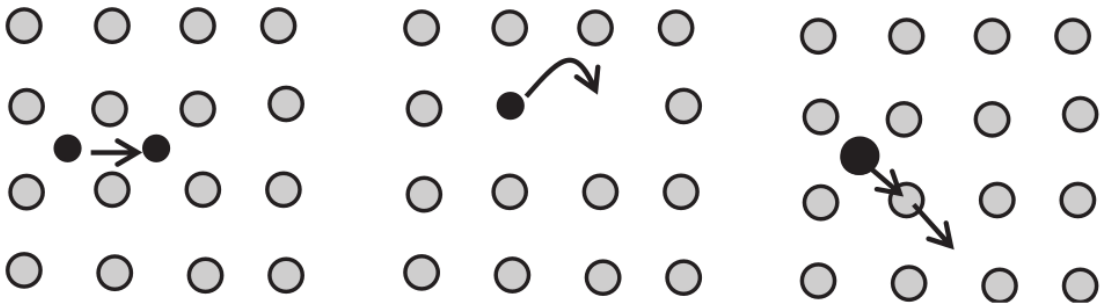


Figure 10: Generally, diffusion can be divided into three different mechanisms: interstitial, substitutional and kick-out, respectively from left to right. [54]

In substitutional diffusion, atoms at normal lattice sites can move to adjacent vacant lattice sites. This is the case at elevated temperatures where the concentration of defects including vacancies is high. In the kick-out mechanism, interstitial atoms move to filled lattice sites by kicking out the atom in the lattice site. This mechanism can generally be observed if the concentration of diffusing atoms is high. [36, 54]

2.3.2 Diffusion mechanism of zinc in GaAs and AlGaAs

Despite the low thermal stability of GaAs and the high temperatures related to diffusion processes, Zn diffusion in GaAs substrates has been extensively studied in 1970–1990. Zinc diffusion in GaAs and AlGaAs can be explained with a combination of dissociative and kick-out mechanisms, but the contribution of each mechanism depends on the substrate material and diffusion conditions, as will be shown in the next few chapters where several models are reviewed. Generally all of the presented models agree that fast Zn diffusion occurs via the interstitial mechanism. Albeit, the slower substitutional mechanism is also present. Fig. 11 illustrates several different species that are participating in the Zn diffusion mechanism in the GaAs crystal, which are typically used in the models explaining the Zn diffusion mechanisms.

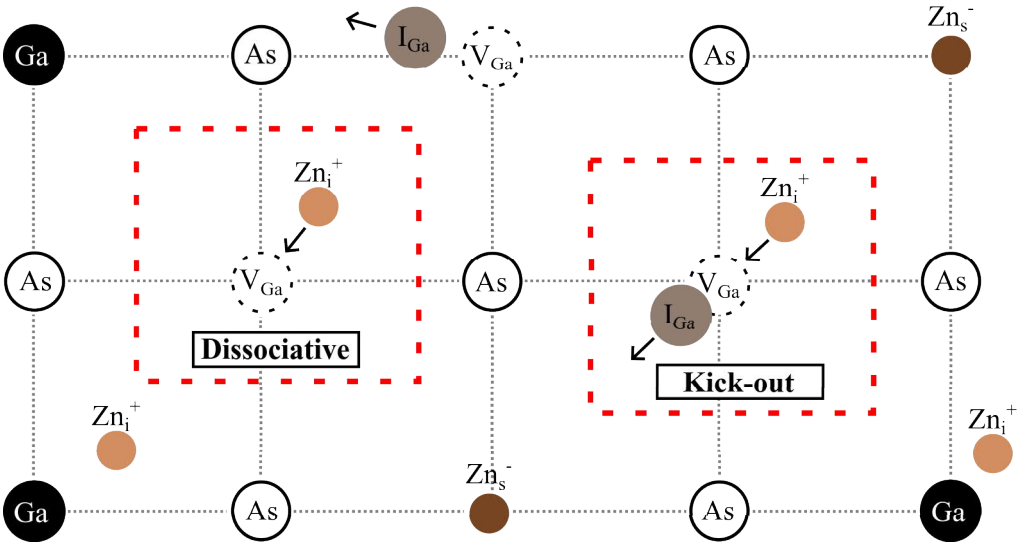


Figure 11: Simplified representation of an arbitrary GaAs crystal plane illustrating dissociative and kick-out diffusion mechanisms, and the ionized Zn species that are involved in the diffusion of Zn in GaAs and AlGaAs. Dashed lines illustrate the bonds between lattice site atoms.

Zinc in GaAs can exist as interstitial $Zn_i{}^+$ ions that are effectively donors. They have released an electron into the conduction band of GaAs, which explains their positive charge. In addition, Zn can exist as substitutional $Zn_s{}^-$ species that are acceptors. They have negative charge since they have received electrons from the GaAs valence band where holes have formed. The interchange process between $Zn_i{}^+$ and $Zn_s{}^-$ is generally described with a Frank-Turnbull mechanism [55]. Other important species are gallium vacancies V_{Ga} and interstitials I_{Ga} that can form due to thermal energy or Zn diffusion.

Longini [56] was one of the first researchers suggesting dissociative mechanism (also known as substitutional-interstitial) to explain the Zn diffusion in GaAs. According to the model, Zn diffuses rapidly as interstitial $Zn_i{}^+$ species. These $Zn_i{}^+$ ions can move into the Ga sub-lattice by filling an already existing gallium vacancy V_{Ga}.

As interstitial $Zn_i{}^+$ ions move to Ga lattice sites, they become $Zn_s{}^-$ ions that are effectively acceptors since they have received electrons from the valence band and thus produced holes h^+ to the valence band. The transition from $Zn_i{}^+$ to $Zn_s{}^-$ is schematically presented in Fig. 11. The dissociative diffusion mechanism follows a quasi-chemical reaction that can be expressed as

$$Zn_i{}^+ + V_{Ga} \rightleftharpoons Zn_s{}^- + 2h^+. \tag{8}$$

The more recent model from Gösele and Morehead [57] proposed a kick-out mechanism for zinc diffusion in GaAs. This is similar to dissociative mechanism in several ways, but the transition from an interstitial $Zn_i{}^+$ to a substitutional $Zn_s{}^-$ is different. While Longini's model [56] is based on the assumption of already existing gallium vacancies in the lattice, Gösele and Morehead suggest that $Zn_i{}^+$ can kick-out gallium atoms and produce interstitial I_{Ga} and Ga vacancies which can then be filled by the $Zn_i{}^+$. This process can be written as

$$Zn_i{}^+ + Ga \rightleftharpoons Zn_s{}^- + I_{Ga} + 2h^+. \tag{9}$$

These models described above successfully explain the base mechanism of zinc diffusion in GaAs. However, they fail to account for unusual characteristics of the process, such as anomalously sharp diffusion front and unusual Zn concentration profiles.

It is generally accepted that the diffusivity of interstitial Zn is known to be significantly higher than that of substitutional zinc. The sharp diffusion front of Zn concentration profile in typical diffusion experiments can be explained with the dissociative diffusion mechanism where interstitial zinc diffuses quickly. If $Zn_i{}^+$ species move to substitutional lattice sites faster than the processes crystal can produce more Ga vacancies, the diffusion is limited by the rate of the new Ga vacancy generation that leads to an abrupt diffusion front. [57, 58]

Ye *et al.* [47] studied the effect of dopant source to the concentration profiles of Zn in GaAs and observed that Zn diffusion can occur with either dissociative or kick-out mechanism, or a combination of both. Fig. 12 illustrates two Zn concentration profiles based on box and kink-and-tail models that can be found in GaAs depending on the dominant diffusion mechanism. By using a Zn-Ga alloy dopant source, a box shaped doping profile can be observed. In this case, gallium rich diffusion conditions hinder the escape of Ga atoms from the sample surface which further hinders the formation of Ga vacancies deeper in the sample. This reduces the possibility of the dissociative diffusion mechanism that happens via Ga vacancies, thus making the kick-out mechanism dominate the Zn diffusion.

A kink-and-tail profile can be obtained when pure a Zn source is used. Higher Zn concentration close to the surface is explained with Ga atoms that can diffuse to the surface and escape the sample which leads to an increased number of gallium vacancies. This enables fast Zn diffusion via the dissociative mechanism that requires Ga vacancies. However, as the depth increases, the number of interstitial Ga atoms that can reach and escape the surface decreases. Consequently, the number of Ga vacancies decrease and at some point the dominant diffusion mechanism changes from fast dissociative to slow kick-out, which explains the tail part of the concentration profile. [47]

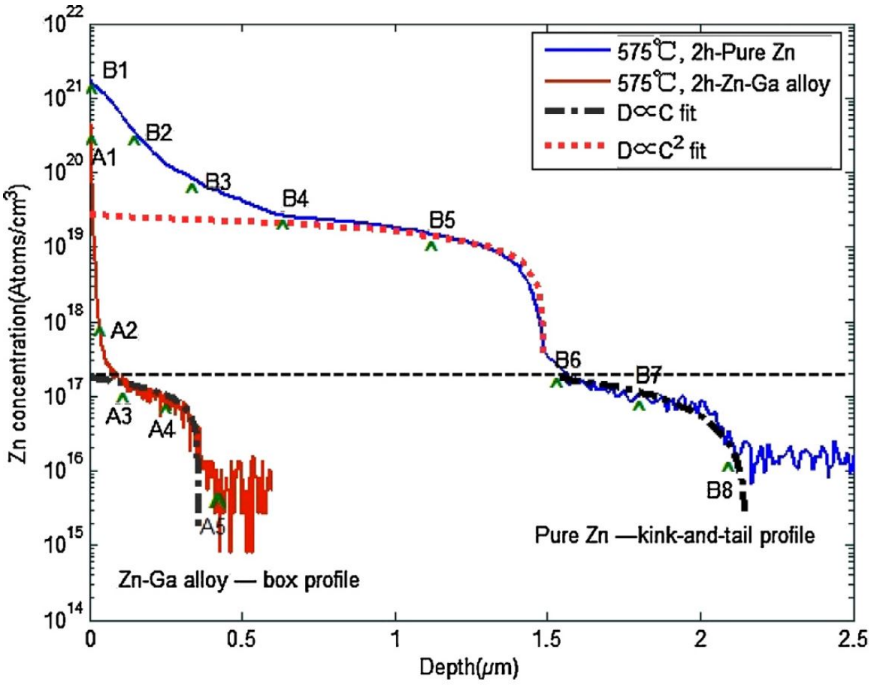


Figure 12: Concentration of Zn in GaAs as a function of depth after annealing for 2 h at 575°C. Also, lines of the best fit are shown. Kink-and-tail profile for a pure Zn source and box profile for a Zn-Ga source are observed. [47]

It has been observed that the diffusion constant of Zn is proportional to the concentration of zinc. Generally, this relation can be described with the following equations

$$D \propto {C_{Zn}}^2 \text{ (Dissociative)} \tag{10}$$

$$D \propto C_{Zn} \text{ (Kick} - \text{out)} \tag{11}$$

where D is diffusion coefficient and C_{Zn} is the concentration of Zn. Eq. (10) can be observed when Zn diffuses with dissociative method [47, 57, 59, 60], and Eq. (11) when diffusion occurs via kick-out mechanism [47, 60].

Fig. 13 illustrates another explanation for the kink-and-tail profile that is based on different ionization states of interstitial zinc that diffuse with the dissociative mechanism. Reynolds *et al.* [60] proposed that the high concentration area of the kink region is caused by doubly ionized interstitials ${Zn_i}^{++}$ that have smaller diffusivity than singly ionized ${Zn_i}^{+}$. Their model assumes that the energy level of ${Zn_i}^{++}$ is roughly 0.2 eV above the valence band edge and that singly ionized interstitials ${Zn_i}^{+}$ have a higher energy level close to the center of the GaAs band-gap. During diffusion, close to the substrate surface where Zn concentration is high, Fermi energy level is close to the valence band edge. Doubly ionized interstitial zinc can exist when the Fermi level is below the energy level of ${Zn_i}^{++}$. As the Zn concentration decreases

deeper in the sample, the Fermi level will increase and thus the $Zn_i{}^{++}$ concentration will quickly drop. After this, diffusion of singly ionized $Zn_i{}^{+}$ with higher diffusivity will form the tail part of the kink-and-tail profile.

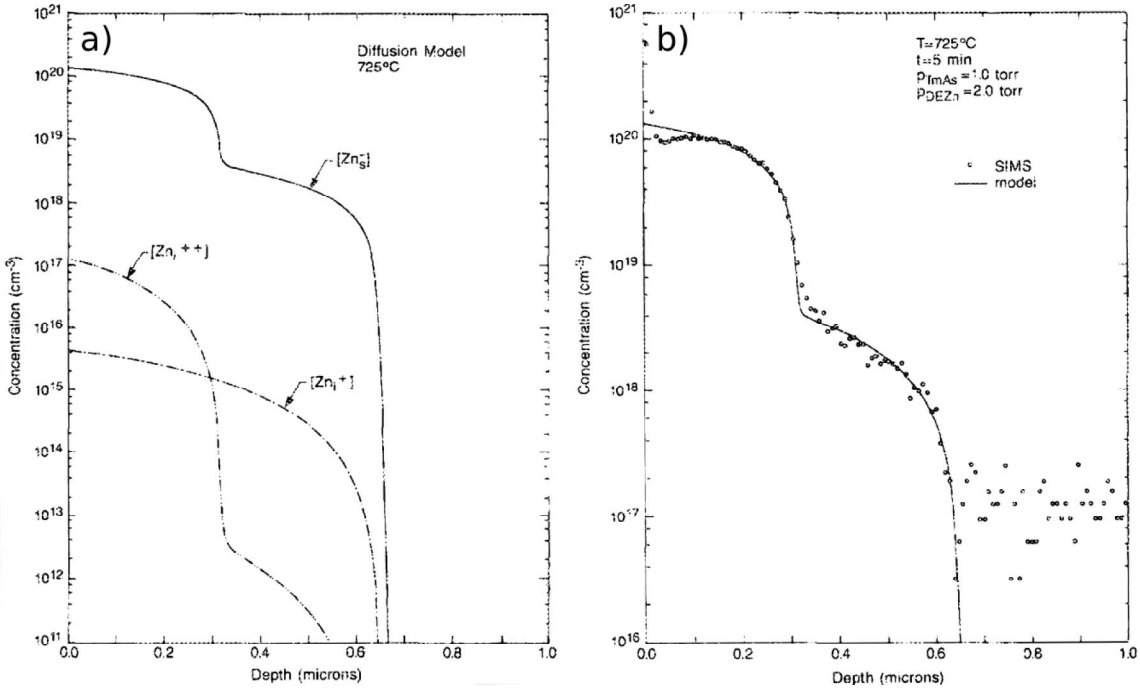


Figure 13: Simulated and measured concentration profiles of different Zn species in GaAs after 5 min of diffusion at 725 °C using diethylzinc and trimethylarsenic sources. (a) Simulated concentration profiles of substitutional $Zn_s{}^{-}$, and singly and doubly ionized interstitial $Zn_i{}^{+}$ and $Zn_i{}^{++}$. (b) Simulated concentration profile of $Zn_s{}^{-}$ is well fitted to the actual Zn concentration profile in the sample measured with secondary ion mass spectrometry (SIMS). [60]

Yet another explanation for the unusual Zn concentration profiles was proposed by Kahen [61]. Instead of using multiple ionization levels for interstitial Zn, Kahen assumed that Ga vacancies have two ionization states $V_{Ga}{}^{0}$ and $V_{Ga}{}^{-}$ that are determined by the position of the Fermi level. In addition, he suggested that pairing between interstitial $Zn_i{}^{+}$ and substitutional $Zn_s{}^{-}$ can form neutral Coulomb pairs. This pairing could hinder the diffusion of mobile $Zn_i{}^{+}$ since the concentration of relatively immobile $Zn_s{}^{-}$ is higher. According to Kahen, this indicates that the diffusion of Zn in heavily doped GaAs is slower than in undoped GaAs. In later studies [51], the model was extended for n-doped substrates. It was suggested that n-doping increases the concentration of the negatively charged $V_{Ga}{}^{-}$ in the substrate which effectively slows down the Zn diffusion by retarding the diffusion of the $Zn_i{}^{+}$.

According to Choudhury *et al.* [62], diffusion of Zn in $Al_xGa_{1-x}As$ occurs with similar mechanisms than in GaAs. However, depending on the Al content in the substrate, the diffusion rate is higher. As Al content increases, the binding energy between Ga, As and Al atoms increases and thus the substitution of Ga atom by

Zn acceptors becomes more improbable. Consequently, a faster interstitial diffusion process becomes more dominant. Fig. 14 illustrates the difference of produced junction depths is GaAs and AlGaAs with different Al contents and Zn diffusion temperatures. These findings are in agreement with the studies of Lawrence *et al.* [63].

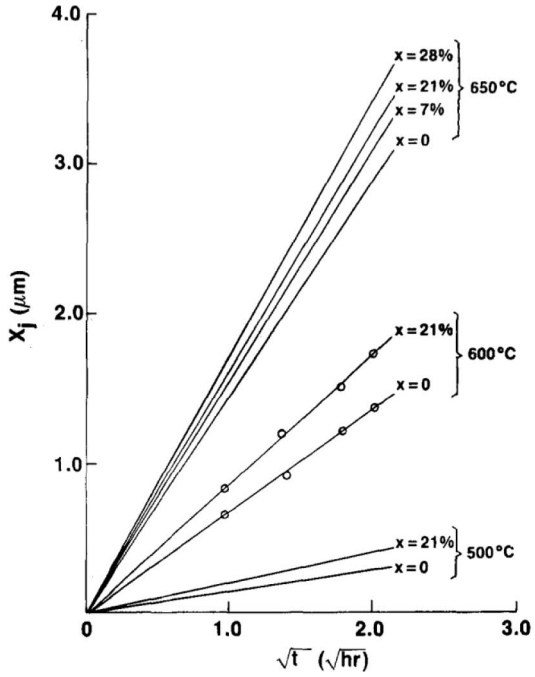


Figure 14: Junction depth in GaAs and AlGaAs as a function of the square root of the Zn diffusion time at temperatures of 500, 600 and 650 °C. The symbol x represents the Al content in AlGaAs. [62]

Chatterjee *et al.* [64] studied how the diffusion mechanism of zinc changes depending on the used cap layer. The PSG cap layer that blocks the out-gassing of both As and Ga atoms, should produce a Ga rich sample and thus a box-like Zn concentration profile. CVD deposited SiO_2 and SOG films would allow Ga out-gassing from the sample and produce an As rich surface region and thus a kink-and-tail profile. These results are in agreement with the research conducted by Jäger [65], who studied the effect of Ga and As rich diffusion conditions. These observations indicate that the cap layer and the used diffusion conditions have a significant impact on the dominant diffusion mechanism and thus the resulting concentration profile of Zn, that might explain the high number of slightly differing models explaining Zn diffusion in GaAs.

2.3.3 Diffusion doping of GaAs

Generally, doping can be performed from gaseous, liquid or solid dopant sources. Diffusion doping is a relatively simple method, but the maximum dopant concentration in the substrate is limited by the solid solubility limit for the dopant atoms. If the dopant concentration is too high, the dopant atoms might form precipitates that cannot contribute to the electrical conductivity. [54] Zn diffusion in GaAs has been conventionally done from either gaseous or solid dopant sources.

Zn diffusion utilizing sealed ampoule techniques has been traditionally the most popular doping method for GaAs and AlGaAs [62, 66, 67, 68, 69]. In this method, a substrate and a solid dopant source are placed inside an ampoule that is evacuated and manually sealed. Then the whole ampoule is heated in a furnace so that dopant source atoms sublimate. Vaporized dopants travel to the substrate and diffuse into it. Sealing of the ampoules ensures saturated vapor pressure which leads to uniform doping and reduced surface damage of the substrate. Additionally, Zn-As, Zn-Ga or Zn-As-Ga alloys can be used inside the ampoule to provide protective As and Ga over-pressures accordingly. This technique has been used to perform successful Zn diffusion doping with high reproducibility. However, the demanding control of As and Ga pressures and the labor intensive sealing of the ampoules makes the method unattractive for commercial fabrication [44].

Zn diffusion with open-tube furnaces has also been a common doping method for GaAs and AlGaAs [60, 70]. In this technique, the substrate is placed in a quartz tube furnace. Dopants are introduced in flowing precursor gases such as diethylzinc. In addition, gaseous As and Ga species, or carrier gases like N_2 or Ar can be used to prevent the thermal decomposition of the substrates. Although good and reproducible results can be achieved, highly toxic As gases make these processes unattractive for most purposes.

Doping from solid dopant sources such as Zn and ZnO thin films, SOG films, and CVD deposited dielectric films is generally more straightforward compared to diffusion from vapor phases. Solid dopant sources are first deposited on the substrate surface and then as samples are annealed, dopant atoms are driven into the substrate. The advantage of this method is that the solid film can simultaneously function as the dopant source and a protective cap layer which reduces the need for other protection. Generally, annealing in open-tube furnace with flowing N_2 or Ar gases is enough for successful Zn diffusion, and thus the use of Ga and toxic As rich diffusion conditions can be avoided. Furthermore, lower process temperatures can be used, since there is no need to maintain high vapor pressures of dopant atoms.

First studies utilizing solid Zn sources were done by Goldstein [71] who used an electro-deposited Zn film as the dopant source in 1960. He performed diffusion doping of GaAs substrates at temperatures below 800 °C, and found out that the observed Zn concentration $C_{Zn}(x)$ profiles followed the solution of

$$C_{Zn}(x) = \frac{Q_{Zn}}{\sqrt{\pi D t}} \exp\left(\frac{-x^2}{4Dt}\right), \tag{12}$$

where Q_{Zn} is the amount of deposited Zn (at/cm^2), D is the diffusion constant, t is the time and x is the depth. Although, good results were achieved by Goldstein, some problems with the zinc dopant sources remained. Only some of the specimens were successfully doped because the zinc films evaporated from the substrate surface so that only a small amount of Zn actually diffused into the substrates. However, 800 °C is a relatively high temperature for Zn films, and no reported efforts were spent to protect the zinc film or the substrate by Goldstein.

More advanced diffusion from zinc oxide thin films was researched by Sakai *et al.* [72] nearly 20 years later in 1978. A 50 nm thick evaporated zinc thin film was deposited on a n-type GaAs wafer, and then anodized to produce ZnO, which is thermally more stable compared to elemental zinc. Diffusion annealing in an open-tube furnace under nitrogen flow produced good results, where the junction depth x_j followed Chang's equation [73]

$$x_j = D_0\sqrt{t}\exp\left(\frac{-E}{kT}\right). \tag{13}$$

In the past 40 years, Zn diffusion from doped cap layers such as SOG and CVD deposited SiO_2 films have become more popular. The advantage of these methods is that the cap layers function simultaneously as the dopant source and the protective layer. Due to this, open-tube processes with flowing N_2 or Ar gases can be used to obtain successful Zn doping, and thus the use of Ga and toxic As rich diffusion conditions can be avoided.

Zn diffusion from doped SOG films has been investigated in several studies [42, 74, 75] in 1980–1992 and also recently in our group [26]. Typically, SiO_2:ZnO SOG dopant source is first spin-coated on the substrate which is then annealed under a protective atmosphere to drive the dopant atoms into the substrate. In addition to silica based films, a ZrO_2:ZnO dopant source that should have higher stability has been demonstrated [76].

The use of doped SiO_2 films deposited with CVD has also been used for Zn diffusion doping [43, 44, 45, 63]. These methods use often undoped cap layers such as SiO_2 or phosphosilicate glass (PSG) on top of the dopant source to provide extra protection. For example, Lawrence *et al.* [63] used metal-organic chemical vapor deposition (MOCVD) grown Zn-doped SiO_2 as a dopant source. Additionally, protective undoped SiO_2 film was deposited on top of the dopant source and the backside of the substrate. P-doped areas with abrupt diffusion fronts were achieved in n-GaAs substrates after diffusion at 650 °C under N_2 ambient. Fig. 15 represents zinc concentration profiles observed by Lawrence.

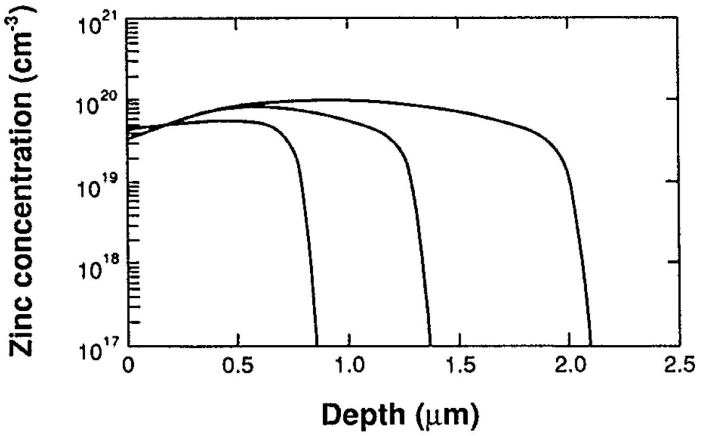


Figure 15: Concentration profiles of Zn in n-GaAs, using a MOCVD grown Zn doped SiO_2 dopant source with 71 wt% of Zn. Diffusion was performed at 575 °C for 15, 30 and 60 min (from left to right), and the concentration was measured with SIMS. [63]

2.3.4 Ion implantation

Ion implantation is another doping process used in semiconductor technology. It utilizes accelerated ions hitting and penetrating into the substrate. High implantation energies of 10–200 keV are used depending on the dopant atom. Implantation depths are typically at the range of hundreds of nanometers. [54] Compared to vapor phase diffusion, ion implantation is an attractive method due to its fine control over doping profile and reproducibility [77].

The disadvantage of ion implantation is that it causes damages to the substrate material. Because of this, a high temperature annealing step is required to remove such damages. This annealing is difficult with III-V materials due to their low thermal stability. Especially in the case of light emitting devices where defect free materials are important, the use of ion implantation as a fabrication method is rather complicated. For example, damage annealing for GaAs substrates typically requires temperatures from 700 °C to 900 °C [77, 78]. To prevent the evaporation of As and possibly the implanted atoms (e.g. Zn), a capping layer is needed for the annealing step. For example, a silicon nitride film can be deposited on the substrate with either CVD or sputtering. Depending on the deposition method and layer thickness, different doping profiles can be achieved. [78]

Boissy and Diquet [77] obtained good results of implanting zinc atoms into GaAs. They carried out implantation through a 70 nm thick nitride film which was later used as a capping layer during annealing. Using the same nitride layer in both steps produced better results due to a large concentration of zinc also in the capping layer. They suggested that zinc atoms in the capping layer enhances the protective properties of the film.

Regardless of the problems related to ion implantation into compound semiconductors, selective-area Si implantation into p-GaN to produce DDCT like LEDs has recently been demonstrated by Lee *et al.* [25]. They successfully utilized lateral p-n junctions at the top layer of GaN as a carrier injector for InGaN/GaN multi-quantum wells located below the implanted GaN layer.

Although, the materials used by Lee *et al.* are completely different compared to the GaAs/AlGaAs DHJ structure suggested by us, the working principles of their device is very close to our DDCT devices. However, the viability of selective-area implantation for GaAs based DDCT devices is not known. The need for a separate implantation process with a mask and annealing steps combined with a capping layer, makes ion implantation rather complicated. Therefore, simpler diffusion methods were chosen for this thesis.

2.4 Lateral device doping

For the fabrication of lateral devices such as DDCT LEDs, more advanced methods are needed. One possibility is to use spatially resolved selective doping with either diffusion or ion implantation methods that were reviewed in the previous chapter. Additionally, selective-area growth methods can be generally used.

2.4.1 Selective doping

Selective-area doping can be achieved by several methods depending on the doping method and the dopant source. Several different strategies can be used with selective diffusion doping while ion implantation is mostly limited to hard masks. Some of the most common strategies are illustrated in Fig. 16.

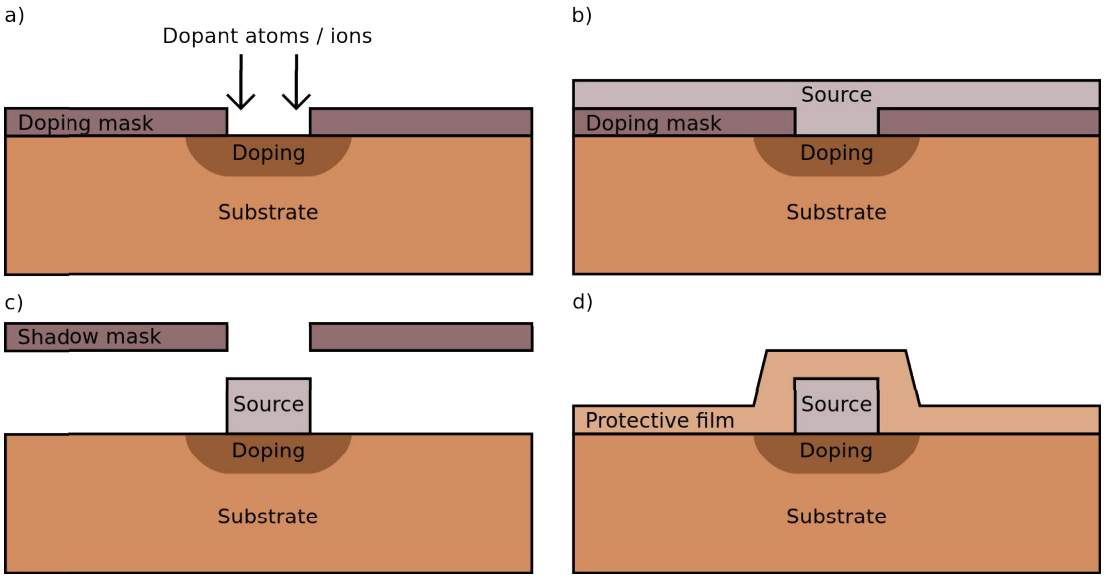


Figure 16: Selective doping methods. (a) Doping mask can be used with ion implantation or diffusion from a gaseous source. (b) Additionally, solid dopant sources such as SOG can be deposited on top of the mask. (c) Dopant sources such as metallic thin films can also be deposited through a shadow mask. (d) An additional film such as SOG might be required to protect the sample surface during diffusion annealing.

Selective diffusion doping from a gas phase can be done with a hard mask such as silicon nitride or a thick silicon oxide mask. The mask is first deposited on the substrate surface and then patterned with conventional lithography and etching processes. When the diffusion is performed, the mask will protect the substrate, and thus only the unmasked areas will be doped. Fig. 16(a) illustrates this possibility. A similar strategy can also be used with ion implantation. In this case, a photo-resist mask is generally adequate. [54]

When solid dopant sources are used, more options are available for selective doping. Similar masks that are used with gaseous dopant sources can be used also with solid sources. Fig. 16(b) represents a situation where a dopant source film is simply deposited on top of the masked substrate, so that only the unmasked parts are doped during diffusion. Additionally, the dopant source itself can be patterned with lithography and etching processes or by depositing the source film through a shadow mask as illustrated in Fig. 16(c). If III-V or other compound semiconductors are used, the substrate surface with the patterned dopant source should be covered with a protective cap layer, illustrated in Fig. 16(d), to prevent decomposition of the surface.

One additional aspect that has to be considered in the mask designs with selective doping, is the sideways spreading of the diffusing atoms. The doped area cannot be strictly restricted by the mask, or patterned dopant source, since the dopant atoms are diffusing also in the lateral direction. Generally, the sideways spread is worse for diffusion doping than for ion implantation. As a rule of a thumb, the ratio of sideways spread to diffusion depth is 1:1 for diffusion doping and 1:3 for ion implantation. [54]

2.4.2 Selective-area growth

Selective-area growth is an epitaxial growth process, which enables separately grown n- and p-regions on a same substrate. SAG is not exactly a doping process, but since dopant atoms can be added into the material during growth, it is one of the alternative options for diffusion doping and ion implantation. In SAG, openings in a patterned mask layer on the substrate surface is used to determine the areas where growth will occur. Selective-area growth of lateral GaN is presently studied in our group [15].

SAG of GaAs and GaAs/AlGaAs multilayer structures is also technically possible, and some studies about SAG of intrinsic GaAs layers have been done. In 1977, Tsang and Ilegems [79] demonstrated selective-area growth of GaAs/AlGaAs multilayer structures with an MBE setup using a patterned Si shadow mask that was pressed against the GaAs substrate. A couple of years later in 1984, Ghosh and Layman [80] used MOVPE to selectively grow GaAs on a (100) GaAs substrate that was masked with a conventional SiO_2 film. They got good results with a substrate temperature of 680 °C where the growth of GaAs took place only on the unmasked substrate. In 1990, Hiratani *et al.* demonstrated selective area growth of GaAs with metal-organic MBE by using GaAs oxide mask that was patterned with electron beam lithography (EBL) [81]. Similar process with EBL patterned GaN mask was researched a few years later in 1994 by Yoshida *et al.* [82].

Only a few studies about SAG of doped GaAs layers can be found. In 1993, selective-area growth of p+-doped GaAs contact layers with laser-assisted atomic layer epitaxy was studied by Chen *et al.* [83]. One year later, Bove *et al.* [84] demonstrated SAG with chemical beam epitaxy of n-GaAs layers with a silicon concentration of 2×10^{18} cm^{-3} to fabricate source and drain for high electron mobility transistors. In 1999, Yokoyama *et al.* [85] demonstrated selective area growth of n-GaAs by a low-pressure MOVPE and achieved a silicon concentration of 5×10^{18} cm^{-3}. More recent studies of SAG of a doped GaAs layers were not found, although n-GaAs nanostubs were recently researched by Chang *et al.* [86]. Generally, the small amount of available studies about selective-area growth of intrinsic and especially doped GaAs layers indicates that the process is still extremely demanding and challenging.

3 LED device physics

Understanding device physics and the internal processes of LEDs is crucial for interpreting the results of the experimental studies and device simulations described later in this thesis. Additionally, this understanding can be used to plan future actions and determining the limitations and possibilities of the studied devices. Here, a simplified view of the formation and operating principles of a p-n junction diode are first introduced, by considering only the effect of charge transport and radiative recombination. Then, a more general view of the most important recombination processes for LEDs are briefly reviewed. Additionally, conventional DHJ and novel DDCT structures are explained and compared. Finally, Schottky barriers and conventionally used ohmic contacts for GaAs systems are discussed. In Section 4, some of these theories are used to simulate new GaAs/AlGaAs DDCT LEDs.

3.1 PN-junction diode

The p-n junction is one of the basic building blocks for several semiconductor and optoelectronic devices, including solar cells, LEDs, lasers, photo-detectors and transistors. It is formed when p- and n-doped regions are interfacing one another. Generally p-n junctions are fabricated during the epitaxial growth processes or by selectively doping parts of a doped semiconductor substrate with the opposite doping type. In the latter case, one of the doping processes reviewed in Subsection 2.3 can be used for this. Fig. 17 illustrates the formation of a p-n junction starting from the energy levels associated with separated n- and p-doped materials.

Fig. 17(a) represents the most significant energy levels present in separate n- and p-doped materials when they have no electrical interaction. In the n-doped material, positively charged donor atoms have released electrons into the conduction band of the semiconductor, and thus electrons are the majority carrier type and the Fermi level is close to the conduction band edge. In the p-doped material, acceptors have received electrons from the valence band where holes have formed, and thus holes are majority carriers and the Fermi level is close to the valence band edge. Additionally, some holes exist in the n-type material and electrons in the p-type material as minority carriers. [87]

In Fig. 17(b), p- and n-doped materials are allowed to equilibrate. Due to a high concentration difference of charge carriers between the two sides of the junction, a diffusion current of free electrons from n-side towards p-side and free holes from p-side towards n-side starts. When these mobile charge carriers meet at the interface, they effectively cancel each other, and so the concentration of electrons and holes close to the p-n junction decreases. Consequently, immobile charges of ionized donors and charged acceptors are left at the interface, so that a potential difference called diffusion voltage V_D is formed. For non-degenerate junctions, the diffusion voltage can be calculated with

$$V_D = \frac{kT}{q} \ln\left(\frac{N_A N_D}{{n_i}^2}\right), \tag{14}$$

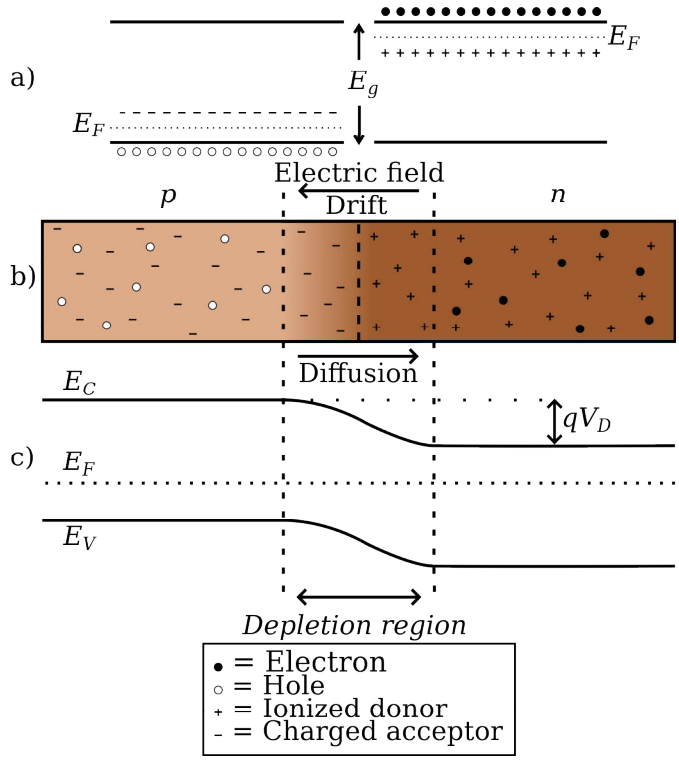


Figure 17: Formation of a p-n junction. (a) Separated n- and p-doped materials. (b) When these materials are joined a depletion region will form due to the carrier drifting and diffusion. (c) Band diagram of the formed p-n junction in equilibrium.

where k is the Boltzmann constant, T is the temperature, q is the elementary charge, N_A and N_D are the donor and acceptor concentrations, respectively and n_i is the intrinsic carrier concentration of the semiconductor.

A drift current of charge carriers opposing the diffusion currents is now caused by the electric field generated across the junction. As the drift and diffusion currents are equal, the junction is at equilibrium, where the diffusion voltage represents a barrier that a free charge carrier must overcome in order to move across the depletion region. This kind of a junction is called a p-n junction diode, since the potential barrier across depletion region allows current flow primarily in one direction. The threshold voltage V_{th} where a non-neglible current starts to flow through the diode is typically of the order of V_D for non-degenerate junctions, and generally lower than the band-gap energy of the diode material divided by the elementary charge q as expressed with the following expression [37, 50, 87]

$$V_{th} < V_D < E_g/q. \tag{15}$$

Fig. 17(c) represents the band diagram of the formed p-n junction at zero bias. When the n- and p-doped parts are in equilibrium, the Fermi level across the whole junction must become constant. This leads to band bending of the conduction and valence bands, due to the difference between the Fermi levels of separate n- and p-doped regions shown in Fig. 17(a). [87]

If a bias voltage is applied on the p-n junction so that it opposes the built-in diffusion voltage in the depletion region, the junction is forward biased. This means that the barrier introduced by the diffusion voltage decreases so that charge carriers can move across the junction. Simultaneously, the width of the depletion region decreases and the carrier population in the conduction and valence bands becomes unbalanced near the junction. As electrons and holes are injected into the region with opposite doping they recombine primarily by emitting a photon, if a direct semiconductor material is used to create the p-n junction. Other recombination processes discussed in the next Subsection are also present. This is the basic operation principle of LEDs, which are fundamentally p-n junctions. [37]

If the applied bias voltage is reversed so that it increases the barrier height, the junction is reverse biased. In this case, only few thermally excited carriers can move across the junction which results in a small leakage current. At a high reverse bias, a junction breakdown will occur with either avalanche or Zener mechanisms. A typical mechanism in moderately doped junctions is the avalanche breakdown where a high electric field can raise some of the electrons from the valence band into the conduction band. In this process called impact ionization, electron-hole pairs are generated which leads to increased current flow through the avalanche effect. Zener mechanism occurs generally in heavily doped junctions with narrower depletion region. In this case, electrons can tunnel through the depletion region when the reverse bias is high enough. [88]

3.2 LED current and carrier distribution

Fig. 18 represents the IV-curve of an ideal diode on linear and logarithmic current axes. When a linear axis is used, V_{th}, I_0 and the breakdown regions are clearly visible. The logarithmic I-axis can be used to study the internal processes of the diodes.

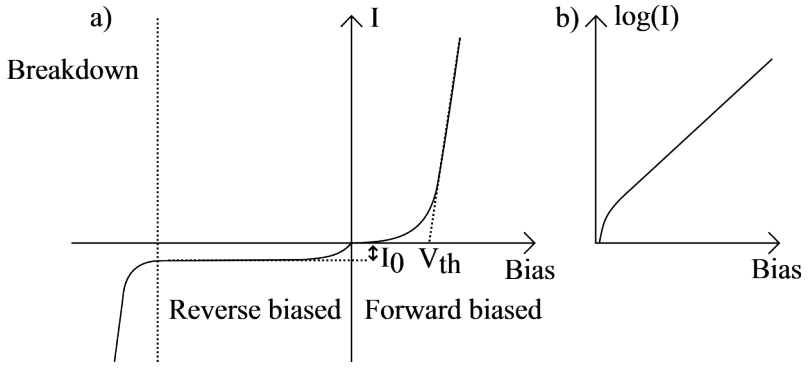


Figure 18: Qualitative illustration of the regions of the current-voltage curve of an ideal diode. (a) The forward and reverse bias regions, the junction breakdown at higher reverse bias, the reverse saturation current I_0 used in the Shockley equation and the threshold voltage V_{th} of the diode. (b) Logarithmic I-axis can be used to determine ideality factor of the diode and to evaluate its internal processes.

The current flow through a forward biased p-n diode shown in Fig. 18(a) or an LED can be estimated with the Shockley equation

$$I = I_0 \left[\exp\left(\frac{qV}{mkT}\right) - 1\right], \tag{16}$$

where I_0 is a reverse saturation current, V is the bias voltage and m is the ideality factor of the diode that is unity ($m = 1.0$) for a perfect diode or an LED. For real devices m is generally in the range of 1.1–2.0, although much higher values have been reported for AlGaN/GaN diodes [89]. At high bias voltages where $V \gg kT/q$, Eq. (16) can be re-written as

$$I = I_0 \exp\left(\frac{qV}{mkT}\right). \tag{17}$$

The logarithmic I-axis, shown in Fig. 18(b), is generally also used, since it can be used to estimate the internal processes of the diode. The slope of the linear region of log(I)-V curve can be used to obtain the ideality factor of the diode. If a logarithm is taken of Eq. (16) the current on log-scale is given by

$$\log(I) = \left(\frac{q}{mkT}\right)V + \log(I_0), \tag{18}$$

where q/mkT corresponds to the slope of the linear region. In addition to the ideality factor, Eq. (18) can be used to estimate the internal processes of the diode such as Shockley-Read-Hall recombination that will be discussed in the next Subsection.

In more microscopic terms, forward biasing an LED leads to a very large increase in the minority carrier concentration near the p-n junction. At thermodynamic equilibrium for which $np = {n_i}^2$, the distribution of electrons follows the Fermi-Dirac distribution given by

$$f_e(E) = \frac{1}{\exp\left(\frac{E-E_F}{kT}\right) + 1}, \tag{19}$$

where E_F is the Fermi level. If $E - E_F \gg kT$ the carrier distribution is called non-degenerate and the electron distribution can be approximated by the Boltzmann distribution

$$f_e(E) \approx \exp\left(-\frac{E - E_F}{kT}\right). \tag{20}$$

Carrier concentrations for non-degenerate semiconductors can then be approximated with

$$n \approx N_c \exp\left(\frac{E_F - E_C}{kT}\right) \tag{21}$$

$$p \approx N_v \exp\left(\frac{E_V - E_F}{kT}\right). \tag{22}$$

In a non-equilibrium situation where the diode is externally excited by electric bias, light or carrier injection, a constant Fermi level throughout the structure cannot exist anymore. Instead, the situation can usually be well approximated by assuming that conduction and valence band are internally in equilibrium. This can be described by assigning independent and position dependent quasi-Fermi levels E_{Fn} for CB and E_{Fp} for VB. With quasi-Fermi levels, electron and hole concentrations can expressed as

$$n = N_c F_{1/2}\left(\frac{E_{Fn} - E_C}{kT}\right) \tag{23}$$

$$p = N_v F_{1/2}\left(\frac{E_V - E_{Fp}}{kT}\right), \tag{24}$$

where $F_{1/2}$ is the Fermi integral of the order 1/2. If the quasi-Fermi level is inside the band-gap and energy difference to the band edge is more than $\sim kT$, $F_{1/2}$ can be approximated by [49]:

$$F_{1/2} = \exp\left(\frac{E_F - E_C}{kT}\right). \tag{25}$$

3.3 Recombination processes

Radiative recombination of electrons and holes producing photons in diodes is the fundamental mechanism on which the solid state lighting and LEDs are based on. In the simplified example of an ideal diode that was discussed in previous Subsection, only radiative recombination was considered. In real devices, other processes such as Shockley-Read-Hall (SRH), Auger and surface recombination are also present. These mechanisms lead to non-radiative recombination where photons are not emitted. To understand the internal processes of diodes these recombination mechanisms are briefly reviewed below. Fig. 19 illustrates the radiative, SRH and Auger recombination processes, that are described more closely in the following Subsections.

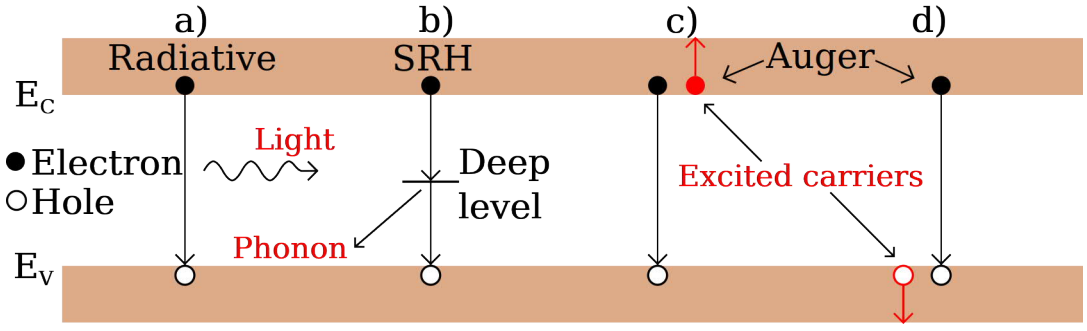


Figure 19: Most typical recombination processes in LEDs. (a) Radiative recombination. (b) Shockley-Read-Hall recombination. Auger recombination for electrons (c) and holes (d).

3.3.1 Radiative

Radiative band-to-band recombination, as shown in Fig. 19(a) occurs when electrons in the conduction band recombine with holes in the valence band emitting photons with an energy equal to the energy difference between electrons and holes. The radiative recombination rate R_{rad} is proportional to both electron concentration n and hole concentration p. The relation between R_{rad} and carrier concentrations can be described with the bimolecular rate equation

$$R_{rad} = B(np - n_i^2), \tag{26}$$

where n_i is the intrinsic carrier concentration of the material and B is the radiative recombination coefficient that has a typical value of 10^{-10} cm^3/s for GaAs. If the LED is not excited, radiative recombination rate vanishes as np becomes equal to n_i^2. [37]

3.3.2 Shockley-Read-Hall

In the non-radiative Shockley-Read-Hall recombination mechanism illustrated in Fig. 19(b), energy is released as heat instead of photons. This process occurs via energy levels located deep inside the band-gap of the semiconductor. Deep-levels can be generated by imperfections in the crystal structure of the material. These imperfections can be caused by dislocations, impurity atoms, interstitials or vacancies of group III and V atoms or by a combination of different defects. These defect traps can capture electrons and holes, and function as recombination centers. [90, 91]

The net SRH recombination rate in non-degenerate semiconductors can be estimated with

$$R_{srh} = \frac{np - n_i^2}{\tau_n(n + n_1) + \tau_p(p + p_1)}, \tag{27}$$

where τ_n and τ_p are SRH lifetimes of electrons and holes, respectively, and n_1 and p_1 are the concentrations of electrons and holes in the case in which the Fermi level of the material is equal to the deep-levels responsible for SRH recombination. [90, 91]

3.3.3 Auger

In Auger recombination shown in Fig. 19 (c) and (d) the excess energy generated in the process is transferred to another electron in the conduction band or to a hole in the valence band. The process can involve several different band valleys when phonons are involved in the recombination process. The Auger recombination rate can be estimated by

$$R_{aug} = (C_n n + C_p p)(np - n_i^2), \tag{28}$$

where C_n and C_p are the Auger coefficient for electrons and holes, respectively.

Strong temperature dependence of Auger recombination can be expressed in Arrhenius [50] form as

$$C(T) = C_0 \exp\left(\frac{-E_a}{kT}\right), \tag{29}$$

where C_0 is the temperature-independent Auger coefficient. Typical Auger coefficients for both holes and electrons in GaAs are in the range of 10^{-31} cm^6/s at room temperature [92]. The probability of Auger recombination increases with high carrier density that can be a result of doping, small band-gap or high current injection. The probability of Auger recombination is proportional to n^2p if two electrons are involved and np^2 if two holes are involved. Eventually, Auger recombination also leads to the heating of the substrate as the energy of the emitted particle is transferred in a non-radiative manner to the lattice. [93]

3.3.4 Surface and interface

Surfaces of semiconductors are a very effective recombination site due to the abrupt break of the crystal lattice that leaves surface atoms with unpaired outer-shell electrons that are called "dangling" bonds. These dangling bonds introduce mid-gap energy levels that function as recombination sites (e.g. traps). The surface recombination rate can be estimated with a recombination current

$$j_s = -qS(n_s - n_i), \tag{30}$$

where S is the surface recombination velocity and n_s is the carrier density at the surface [93]. Typical values of S for bare GaAs surfaces are in the order of 4×10^5 cm/s [92]. Surface recombination of GaAs can be significantly reduced by surface passivation [94].

In addition to surfaces, interfaces between different materials inside the devices can also function as recombination sites, although the interface recombination rates are typically much lower compared to surface recombination. For example the interface recombination rate at GaAs/$Al_xGa_{1-x}As$ interface depends strongly on Al fraction. A value of 450 ± 100 cm/s is typically observed for $x = 0.5$. This is several orders of magnitude smaller than the typical surface recombination rate for GaAs without passivation. [95]

3.4 LED structures

So far the discussion above has considered only p-n homojunctions due to their simplicity. However, this kind of structures are typically not used in real LED devices. Nearly all commercial LEDs and lasers are based on more sophisticated structures such as double heterojunctions where the active region is located between barrier layers that are other semiconductor materials with higher band-gaps [96]. Fig. 20 illustrates a simple DHJ structure and its band diagram under forward bias.

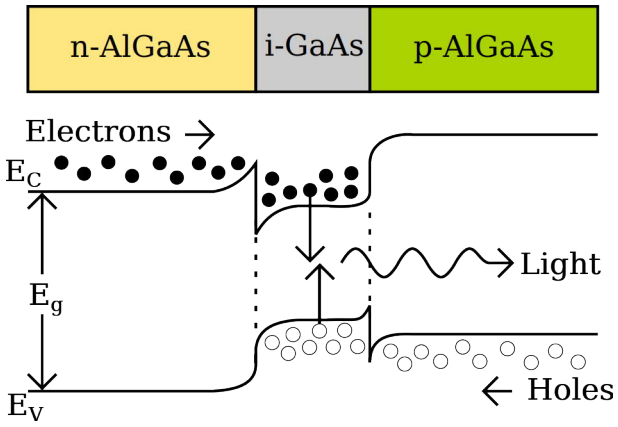


Figure 20: Band diagram of a n-i-p DHJ under forward bias. Electrons are injected from the n-side and holes from the p-side, and both are confined within the intrinsic active layer with a smaller band-gap.

In a typical GaAs/AlGaAs DHJ structure, electrons and holes are injected from the n- and p-sides, respectively. Both charge carriers are confined within the i-GaAs active region due to the potential barriers generated by the AlGaAs barrier layers. This leads to a high concentration of charge carriers within the AR where electron-hole recombination occurs. An additional benefit of the DHJ structure is that the emitted light is not re-absorbed into the barrier layers because the energy of the emitted photons is lower than the band-gap energy of the barrier layers. The DHJ structure shown in Fig. 20 is an ideal vertical LED where the contacts would cover both p- and n-surfaces. This structure is not particularly good for practical LEDs because a significant part of the emitted light is blocked by the contacts.

GaN based structures are generally used in high-efficiency LEDs due to the intense light emission that they can provide in the visible light region. Fig. 21(a) illustrates a typical flip-chip DHJ LED design, where an n-GaN layer functions as current-spreading layer (CSL). In this structure, electrons are injected into the CSL which spreads them under the p-contact mesa. Holes from p-GaN are injected through the i-GaN barrier layer into the AR where recombination with electrons occurs. In this design, light emission downwards has no significant obstacles. While being a viable structure for the needs of most LED applications, this kind of a structure is unideal for high-power LEDs. First of all, the fabrication of the n-contact requires etching through the active region which exposes the edges of the AR for surface recombination. Additionally, this reduces the total volume of the active region which diminishes the amount of radiative recombination. At high input powers, the resistance of the CSL leads to current crowding in the layer, especially at the edge of the n-contact. Current crowding can also be found at the p-contact edge on top of the p-mesa. [14, 15, 37]

Fig. 21(b) illustrates an alternative current injection scheme based on the diffusion driven current transport method which utilizes the diffusion of charge carriers, proposed by our group. These structures are based on the strong diffusion currents and a small band-gap active region collecting the diffusing carriers. This combination

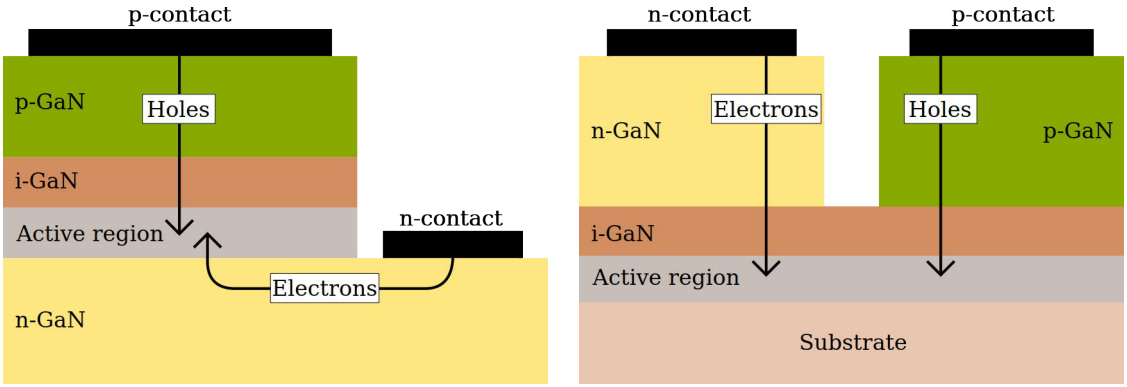


Figure 21: (a) A conventional flip-chip LED structure. (b) A novel DDCT LED structure. The path of injected carriers is illustrated with the arrows.

allows electrical excitation of the AR located outside the p-n junction, as long as the AR is located within the diffusion length of carriers from the p-n junction. This bipolar diffusion method enables the injection of both electrons and holes from the same side of the AR, without the need of etching through the active region. Although promising results with this structure were achieved, the fabrication process including selective-area growth is extremely sensitive to surface contaminations. [11, 14]

Another approach to realizing the DDCT method was suggested very recently by Lee *et al.* [25]. Fig. 22 illustrates the current paths of their structure, in which selective Si-implantation was used to fabricate n-GaN regions. Path A dominated at forward voltages below 15 V, but as the bias was increased, the amount of carriers diffusing into the MQW active region increased significantly. However, the operating voltages of the devices were obviously extremely high. This might be related to the fact that the fabrication of the structure requires ion implantation and

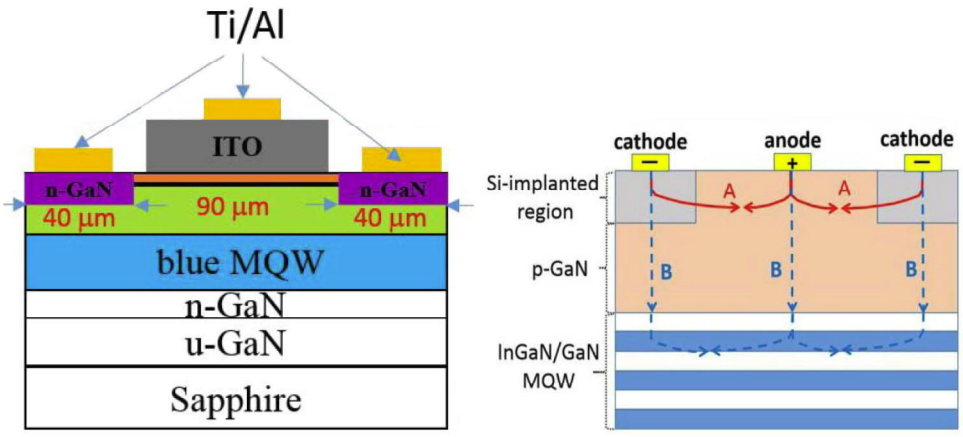


Figure 22: The structure and current paths of blue DDCT injected LED. Path A for the current was observed at low bias, and path B for higher voltages. [25]

damage annealing which is generally not trivial for compound semiconductors, as was discussed in Subsection 2.3.4.

Fig. 23 illustrates the new GaAs/AlGaAs DHJ DDCT structure that is studied in this work. This design utilizes a lateral heterojunction fabricated with selective Zn doping of an n-GaAs buffer layer and the upper n-AlGaAs layer. Electrons and holes are injected into the i-GaAs AR located between the n-AlGaAs barrier layers. This structure and its simulation model are described more closely in the Section 4, and the results of the simulations are shown in Subsection 6.1.

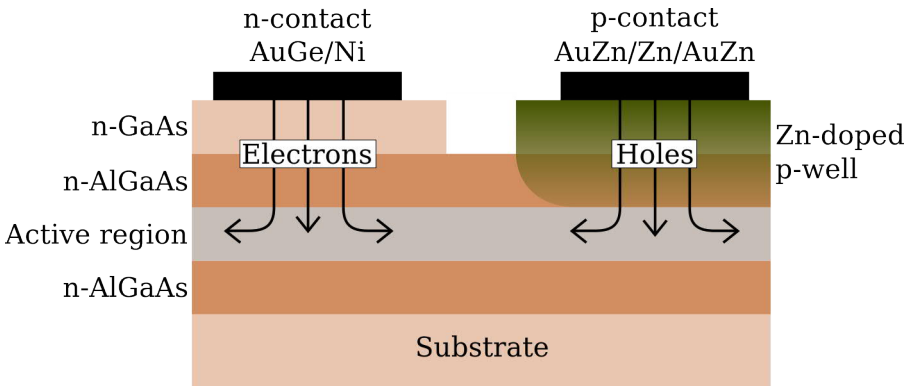


Figure 23: The idealized current injection scheme for a GaAs/AlGaAs DHJ DDCT LED, that enables an unconventional location of AR outside of the p-n junction.

3.5 Contacts for LEDs

Electrical contacts on semiconductor devices are crucially important for both the performance and accurate characterization of the devices. Good electrical contacts provide a linear relationship between current and applied voltage following Ohm's law, and are therefore called ohmic contacts. In addition, the contact resistance should be low to minimize electrical losses.

Contacts are typically manufactured by depositing metal films on semiconductor surfaces by sputtering, evaporating or electroplating followed by a short annealing to allow some diffusion into the semiconductor. The films are generally patterned with standard lithography and etching steps. However, fabrication of ohmic contacts on the surface of GaAs and other III-V compound semiconductors is challenging, due to the high number of surface states that might lead to Fermi level pinning within the semiconductor band-gap. Because of this it is helpful to understand also Schottky barriers that are easily formed at metal-semiconductor (MS) interfaces.

3.5.1 Schottky contacts

When metals are deposited on a semiconductor surface, a Schottky contact with a barrier height Φ_{SB} is easily formed due to the discontinuity in the metal Fermi level ${E_F}^M$ and the band edge of the semiconductor. Ideally, the Schottky barrier height for the MS junction is given by the Schottky-Mott model

$$\Phi_{SB} = \Phi_M - \chi_{SC}, \tag{31}$$

where Φ_M is the work function of the metal and χ_{SC} is the electron affinity of the semiconductor. Eq. (31) provides good estimates for ideal cases, but the model cannot be directly used for gallium arsenide or other III-V compound semiconductors due to the high number of surface states which leads to Fermi level pinning roughly in the middle of the band-gap. These effects lead to a situation where barrier height depends mostly on the semiconductor surface properties and not on the metal work function.

Semiconductor surfaces have a high concentration of surface states due to the dangling bonds as was briefly discussed in Subsection 3.3.4. In addition, it has been proposed that III-V bonds might break during metallization due to the heat-of-condensation released when the evaporated metal atoms condensate on the semiconductor surface. This can lead to the formation of mobile As atoms in GaAs, that produce defects at the MS interface. These defects act as charge carrier traps leading to the pinning of the Fermi level at the trap energy. Since many of these trap energies are within the semiconductor band-gap, the resulting Schottky barrier height at MS junction is typically in the range of 0.7–0.9 eV for GaAs. This pinning mechanism indicates that all metals with a heat of condensation exceeding the bond strength between the surface atoms will have approximately the same barrier height. [97, 98, 99]

Fig. 24 illustrates the formation of a metal-semiconductor junction by representing the energy band diagram of the junction. In Fig. 24(a), the metal and semiconductor are separated. Band bending at the semiconductor-vacuum interface caused by the surface states, can be observed. In this case the pinned Fermi level of semiconductor does not change when the contact is formed in Fig. 24(b) and Fig. 24(c). Consequently, band bending and barrier height are relatively independent of the metal contact.

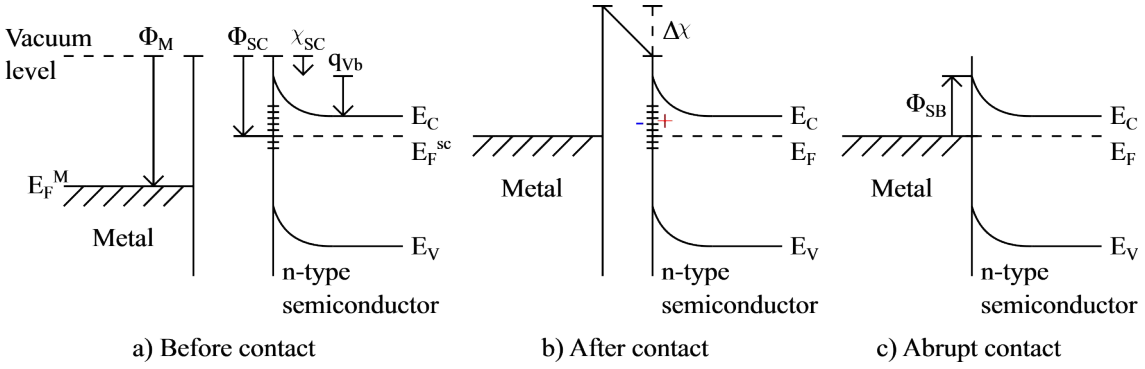


Figure 24: Metal-semiconductor junction energy band diagrams with a high density of surface states leading to pinning of the semiconductor Fermi level. (a) Before contact, the semiconductor band-gap is bent due to the surface states. (b) After contact, a very thin dipole layer between the metal and semiconductor changes the potential difference at the interface leading to spatially abrupt corrections $\Delta\chi$ in the potential profiles. (c) Representation of the typical illustration of the MS junction without explicit inclusion of the interface dipole. [97]

Eq. (31) does not apply for the case in Fig. 24 where significant interface dipoles are formed. Instead the barrier height is approximated with

$$\Phi_{SB} = qV_B + E_C - E_F = \Phi_M - \chi_{SC} - \Delta\chi, \tag{32}$$

where qV_B represents the band bending and the dipole induced change $\Delta\chi$ in the potential depends on the position and density of the surface state energy levels within the band-gap. The formed dipole at the MS interface leads to formation of a capacitive layer with positive charge on the semiconductor side and negative charge on the metal side, as illustrated by the plus and minus signs in Fig. 24(b). [97, 100]

3.5.2 Ohmic contacts

As explained previously, fabrication of ohmic contacts on GaAs surface can be challenging. Thankfully, GaAs devices have been studied for a long time and a few metal combinations have proven to produce good ohmic contacts for these devices. For a p-GaAs surface, multi-layered AuZn/Zn/AuZn [53, 101] contacts have been one of the successful combinations typically used. Here, the first Au layer provides excellent adhesion to the GaAs surface and acts as a nuclei for the intermediate Zn layer. The second Au layer provides protection for the Zn layer during annealing, which lets some of the interlayer zinc atoms to diffuse through the first Au layer into the GaAs. This diffusing Zn provides the ohmic contact with low contact resistance. [101]

Ni/AuGe [53, 102, 103] contacts have traditionally been used for n-GaAs surfaces. In this case, an eutectic AuGe (12 wt% Ge) alloy provides a highly ohmic contact to the semiconductor surface with a low contact resistance. Ni provides surface passivation and improved adhesion for the Au-Ge.

An additional strategy for an n-GaAs surface is provided with InAs [98]. It has been observed that the Fermi level of n-doped InAs is pinned very close to its conduction band. Thus, almost any metal can form a highly ohmic contact with n-InAs. This property can be utilized to make ohmic contacts to other III-V materials if the energy band structures of InAs and e.g. GaAs are matched with intermediate layers. For example graded InGaAs or strained-layer superlattices, can be used as an intermediate layer to gradually change the composition near the MS interface.

Fig. 25 illustrates the energy band diagram of the structure with a heavily doped graded n-InGaAs layer. This structure can be used to produce excellent ohmic contacts without any abrupt interfaces between the layers. The resulting contact is an "ideal" ohmic contact where Φ_{SB} is ≤ 0 eV. However, fabricating the graded $Ga_{1-x}In_xAs$ layer would require epitaxial growth methods such as molecular beam epitaxy. Furthermore, InAs is not suitable for several optoelectronic devices due to its low band-gap energy of 0.354 eV which makes it a very effective light absorber. Thus other methods must be practiced to fabricate the contacts used in this thesis.

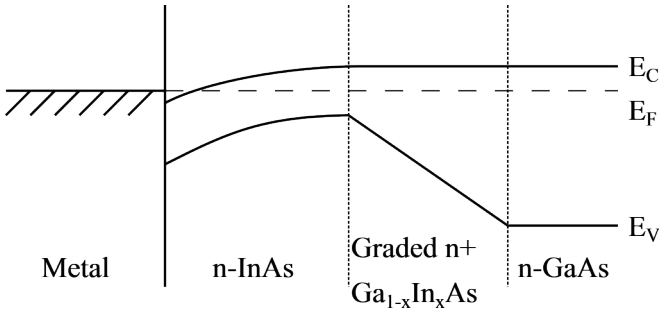


Figure 25: Ohmic contact to n-GaAs via an intermediate n-InAs layer and graded n+ $Ga_{1-x}In_xAs$ layer. [98].

For quick tests and the purpose of this work, elemental indium is also a viable contacting method for, since it provides relatively ohmic contacts to GaAs surfaces and is easily fabricated. Fig. 26 shows a $Ga_{1-x}In_xAs$ interlayer that can be produced by annealing In contacts on GaAs surface to allow some indium diffusion into the GaAs. The composition of the compound can be tuned with the annealing temperature, and $Ga_{0.8}In_{0.2}As$ is achieved at 350 °C [99]. While being inferior to the graded structure in Fig. 25, the structure in Fig. 26 is still able to decrease the barrier height compared to MS junction without any interlayer. This is a result of dividing the large barrier at the MS interface into two smaller barriers at metal/$Ga_{1-x}In_xAs$ and $Ga_{1-x}In_xAs$/GaAs interfaces. Fig. 26 illustrates also how the amount of In decreases closer to the GaAs, increasing also the band-gap energy of the $Ga_{1-x}In_xAs$. [104, 105]

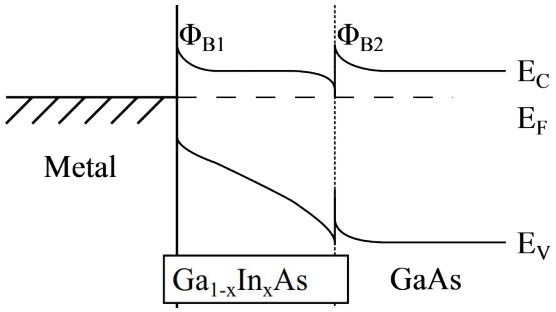


Figure 26: Decreasing of the Schottky barrier height by dividing the barrier in two parts by annealing In contacts on a GaAs sample [104, 105].

The most general strategy for forming ohmic contacts is, in principle, to use highly doped semiconductors at the MS interface because increased doping concentrations decrease the width of the depletion region formed at MS junction. With sufficiently narrow junctions, electrons are able to tunnel through the narrow depletion region. By doing this, electrons are basically bypassing the potential barrier induced by the Schottky junction. Simultaneously, as the doping concentration of the semiconductor increases, the Fermi level within the band-gap gets closer to the valence or conduction band edge. This effectively reduces the barrier height at the metal-semiconductor interface. However, using this approach requires extremely high doping concentrations, which are not always technically feasible. [36]

4 Device simulations

Computational simulations are a very useful tool when designing semiconductor devices, since they can be used to study the internal device operation and the fundamental properties, requirements and limits of the devices. In this work, the goal of the simulations was to evaluate the general feasibility of the suggested GaAs/AlGaAs DDCT structures, by first studying the properties and performance of a relatively small reference structure with a total width of 6 μm. After this, the total width of the devices was gradually increased to 30 μm to study how the performance of the LEDs changes. In this Section, a detailed description of the simulated device is first provided after which the main aspects of the simulation method are briefly described. More detailed information about the model can be found in references [106, 107, 108]. The results of the simulations are provided later in Subsection 6.1.

4.1 Simulated DDCT structure

Fig. 27 illustrates the simulated reference device consisting of a GaAs/AlGaAs DHJ capped with a thin GaAs contact layer. The contact layer on top of the structure is included in the model because fabricating electrical contacts directly on the AlGaAs surface would be significantly more difficult due to highly reactive aluminum [109]. The lateral p-n junction is formed with the Zn doped p-region extending from the p-contact metal to the active region. The top GaAs layer between the contacts is removed to avoid potential problems with the parasitic small band-gap diode that would otherwise be formed. The simulations were performed in 2D, assuming a 100 μm device length along the corresponding unsimulated axis. For the unsimulated

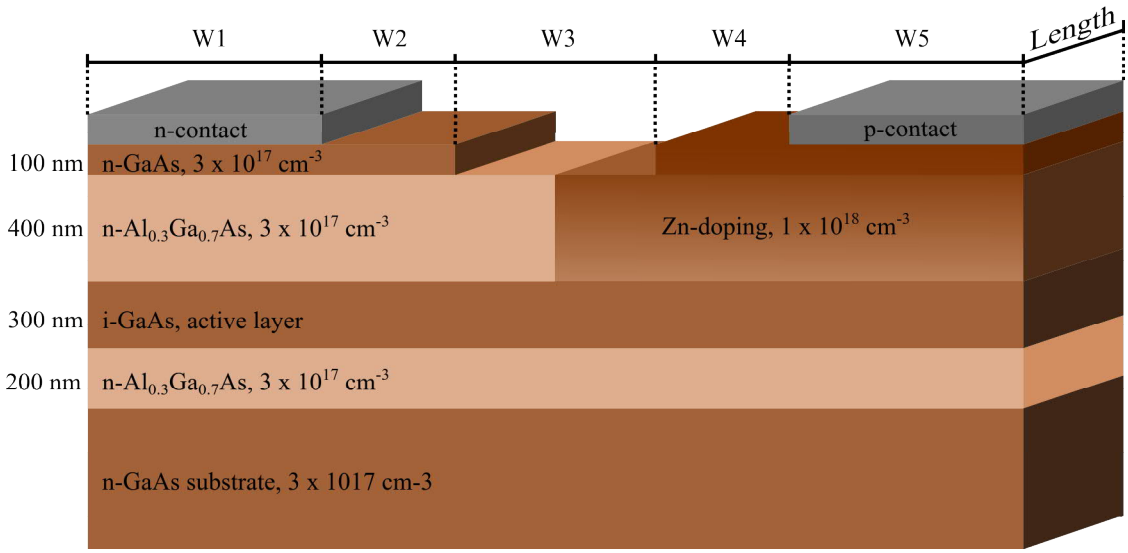


Figure 27: A detailed structure of the simulated DDCT LED device that was used as a reference structure during the simulations. A length of 100 μm was used in the calculations. Sideways spreading of the Zn diffusion was simplified to a square object.

longitudinal dimension, the properties and behavior of the device were assumed to be constant along the corresponding axis. Additionally, the n- and p-contacts shown in Fig. 27 were assumed to be ohmic and lossless.

The structure shown in Fig. 27 should avoid most of the limitations related to flip-chip design, as discussed earlier in Subsection 3.4. The use of lateral p-n junction and the diffusion-driven current transport injection scheme should minimize current crowding at the contact edges. Furthermore, the structure should enable completely new device designs, if the n-GaAs substrate is removed with epitaxial lift-off or some other process.

4.2 Objectives of the simulations

The goal of the simulations was to evaluate the general requirements and limits of the proposed DDCT structure illustrated in Fig. 27. Additionally, the fundamental properties of the simulated devices and the effect of the lateral dimensions W1–W5 on the device operation, such as charge carrier densities and the total recombination rate in different parts of the device, was studied. Because these were the first simulations of the studied structure within the GaAs material system, especially the distribution of charge carriers and the uniformity of the radiative recombination within the active layer were carefully analyzed.

4.3 Semiconductor transport equations

The modeling of carrier transport in bulk semiconductors is typically based on the semiconductor transport equations, which can be derived from Boltzmann's transport equation using several approximations. These simplified transport equations consist of Poisson's equation that is used to model the electrostatic forces and drift-diffusion and current continuity models that are used to approximate the current densities. The model involves solving of the following equations

$$\nabla \cdot (-\epsilon \nabla \phi) = q(p - n + N_d - N_a), \tag{33}$$

$$\nabla \cdot J_n = \nabla \cdot (\mu_n n \nabla E_{Fn}) = qR, \tag{34}$$

$$\nabla \cdot J_p = \nabla \cdot (\mu_p p \nabla E_{Fp}) = -qR, \tag{35}$$

where Φ is the electrostatic potential, ϵ is the permittivity, q is the elementary charge p is the hole density in the valence band, n is the electron density in the conduction band, N_d is the ionized donor density and N_a is the ionized acceptor density. Additionally, J_p and J_n are the hole and electron current densities, respectively, μ_n and μ_p are the electron and hole mobilities, respectively, and R is the net recombination rate per unit volume.

Electron and hole concentrations in the simulations are strongly dependent on the spatial position in the device through their dependence on the electrostatic potential and the Fermi-levels, as described in Subsection 3.2. Together, Eq. (33) – Eq. (35)

form a highly non-linear partial differential equation group that is solved using the finite element method (FEM) solver available in Comsol Multiphysics software.

4.4 Recombination model and parameters

The total recombination term R used in Eq. (33) – Eq. (35) depends on position and is generally given by

$$R = R_{rad} + R_{srh} + R_{aug}, \tag{36}$$

where R_{rad} corresponds to the radiative recombination, R_{srh} to the SRH-recombination and R_{aug} to the Auger recombination that were defined in the Subsection 3.3.

If a homogeneous active region is assumed, Eq. (33) – Eq. (35) can be simplified to produce the familiar form for the current density J through the LED corresponding to the ABC model [93] given by

$$J = qd(An + Bn^2 + Cn^3), \tag{37}$$

where q is the elementary charge, d is the thickness of the active region, n is the excess electron density in the AR, and A, B and C are the SRH, radiative and Auger recombination parameters of the ABC-model, as discussed in Subsection 3.3, respectively.

The ABC-parameters used in the simulations are shown in Table 1. For radiative and Auger recombination parameters B and C, generally established literature values were used. For the SRH recombination parameter A, an experimentally determined value was used. The A-parameter value was very recently determined for one of the structures fabricated and studied by our group, but in literature even smaller values have been reported for GaAs/GaInP DHJ structures [8].

Table 1: The recombination parameters used for the simulations.

Parameter	Value
SRH recombination constant (A)	3×10^5 s^{-1} (measured by the group)
Radiative recombination constant (B)	2×10^{-10} cm^{3}s^{-1} [37, 110]
Auger recombination constant (C)	1×10^{-30} cm^{6}s^{-1} [111]

In addition, the A-parameter can be estimated from experimental IV-measurement data in the SRH-dominated regime using the relation

$$A \sim \frac{J}{qdn_i \exp(\frac{qV}{2kT})}, \tag{38}$$

where J is the current density, d is the thickness of the active region and n_i is the intrinsic carrier density in the AR [19].

4.5 Interpreting the results

Several parameter values are extracted from the simulations. IV-characteristics of the devices are obtained directly from the model by integrating the corresponding net recombination rate over the device volume, then multiplying by q and the cross-section of the contact.

The most important quantities in the context of this work are the recombination rates in the device. They are obtained from the ABC-model once Eq. (33) – Eq. (35) have been solved and the carrier densities are known. The related internal quantum efficiency of the devices is then defined as the ratio between the radiative and the total recombination rates, and is expressed as

$$\mathrm{IQE} = \frac{R_{rad}}{R} = \frac{R_{rad}}{R_{rad} + R_{srh} + R_{aug}}. \tag{39}$$

where all the recombination rates represent average device values, obtained by integrating these parameters through the device volume and then dividing by the volume. Since these simulations are among the very first for this kind of a structure and first for the GaAs based devices, the quantitative ways to define device metrics are not fully established. The current density J used for the simulation results was defined as the integrated total current across the whole structure divided by the total horizontal cross-section area of the device. This is similar to the typical current density representation that is used for the flip-chip design in Fig. 21(a), where the total current flowing through the p-mesa is divided by its surface area.

Additionally, uniformity of the radiative recombination within the active region of the LED was used as a figure of merit. The uniformity was determined as

$$\mathrm{Uniformity} = \frac{\mathrm{Min}}{\mathrm{Max}}, \tag{40}$$

where Max and Min are the maximum and minimum rates for the radiative recombination, respectively. With this definition, a value of 100 % corresponds to a perfect uniformity, and a value of 0 % corresponds to a completely non-uniform situation.

Furthermore, simulation results use radiative recombination rate and carrier concentrations within the active region. Both of these figures of merit are defined as an average value in the vertical direction as a function of lateral position.

5 Materials and methods

In this Section, the samples, fabrication methods and characterization tools used in the experimental studies are described. First, all samples that were used in the experiments are introduced. Then, the evaporation processes and the use of a Zn thin film as the dopant source are discussed. Next, the measures that were used to protect the sample surfaces during diffusion are explained. Then, the etching process that were used to fabricate characterizable p-n diodes are presented. Finally, the metallization of the samples and the characterization methods are discussed.

5.1 Samples and fabrication process overview

Several samples were used during this research. Most of the specimens were cleaved pieces (roughly 1–2 cm^2) of a single side polished silicon doped n-GaAs wafers with a (100) $\pm$ 0.1° orientation acquired from Wafer Technology. The wafers had a diameter of 2" and a thickness of 350 $\pm$ 25 μm. The Si doping concentrations of the wafers were 1.5×10^{17}, 1.0×10^{18} and 2.0×10^{18} cm^{-3}. Additionally, Zn-doped p-GaAs wafers with a doping concentration of $5 \times 10^{18} - 5 \times 10^{19}$ cm^{-3} were used in contact tests. All wafers were used as received from the manufacturer. In addition to bulk wafers, MOVPE grown GaAs/AlGaAs double heterojunction structures and p-n junctions on n-GaAs substrates were used for further experiments and as a reference, respectively. Fig. 28 illustrates the layer thicknesses and doping concentrations of these specimens.

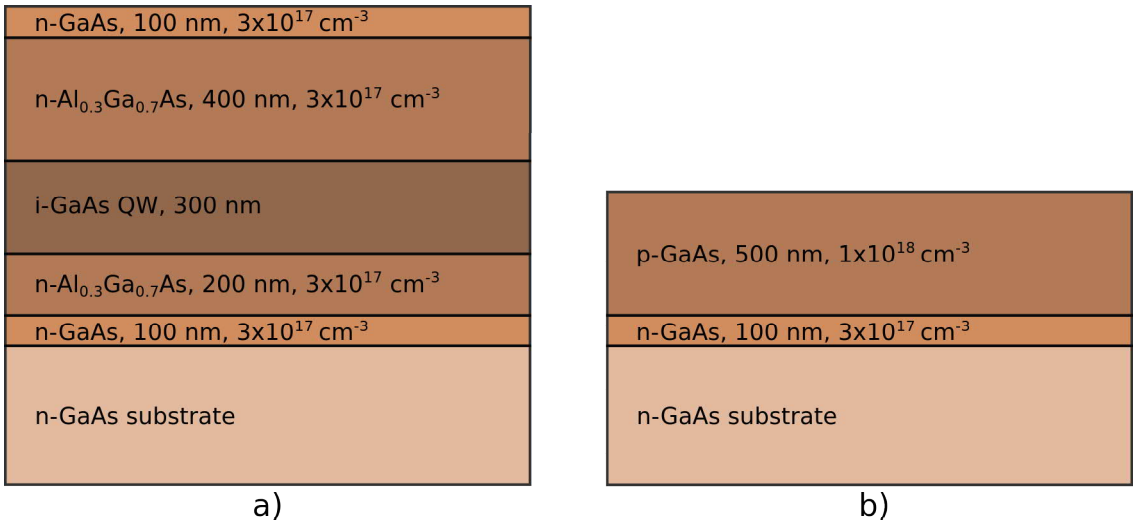


Figure 28: Two types of GaAs substrates with MOVPE grown films were used in this work in addition to plain n-doped GaAs substrates. (a) A GaAs/AlGaAs double heterojunction structure was used to evaluate the feasibility of the diffusion doping process for fabrication of DDCT LEDs with AlGaAs barriers. (b) Epitaxially grown p-n samples were used as a reference for diffusion doped GaAs p-n diodes.

An overview of the developed fabrication process for vertical p-n diodes is represented in Fig. 29. First, a Zn thin film is evaporated on the middle of the sample, and

a protective spin-on glass film is spin coated on the surface of the specimen. Then the samples are placed on top of each other so that processed surfaces are facing each other, and closed inside an aluminum foil and a semi-sealed steel container to provide additional protection. Then the sample stacks are annealed, to allow Zn diffusion into the specimen. Next, sample surfaces are cleaned by removing the SOG film with HF and any remaining Zn with HCl. Then, mesa structures are etched on the sample surface to produce vertical p-n diodes. Finally the diodes are contacted by fabricating a p-contact on top of the surface, and an n-contact to the n-surface at the bottom of the mesas. More detailed descriptions of each processing step and the used characterization tools are provided in the following Subsections.

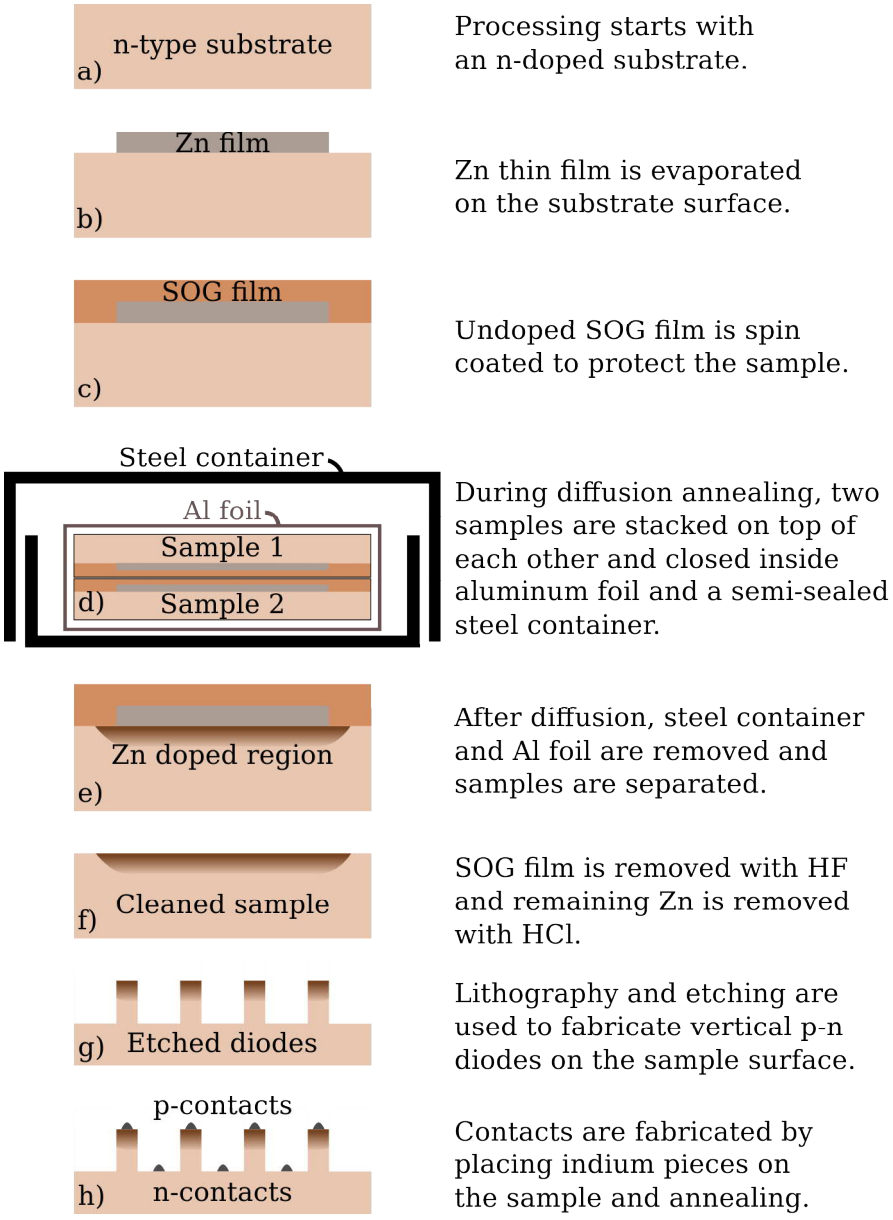


Figure 29: Processing steps for the fabrication of vertical p-n diodes.

5.2 Metal evaporation

Electron beam evaporation was used to deposit the zinc thin film that was used as the dopant source for the diffusion process. The target material for the deposition of elemental zinc was a reeled Zn wire (99.99 % pure). Additionally, Ni/AuGe metal contacts for n-type and AuZn/Zn/AuZn contacts for p-type surfaces were deposited through a shadow mask with the same e-beam evaporator. Two target materials located in the same evaporation chamber were used for these contacts. For n-contacts, an elemental Ni (99.995 % pure) and an eutectic AuGe (12 wt% Ge) alloy (99.99 % pure) were used. Target materials for p-contacts were a AuZn (5 wt% Zn) alloy (99.99 % pure) and the same zinc wire that was mentioned above. Zn source was procured from VWR Chemicals and all of the other sources from Kurt J. Lesker.

In addition to electrical contacts, evaporated zinc thin films were also used as the dopant source for the diffusion process. Zn film thickness of 400 nm was initially used but some tests were also done with thinner films. All depositions were performed with Edwards E306A evaporator around pressures of 1×10^{-6} mbar. Table 2 shows other process parameters for the evaporation of each target material.

Table 2: Parameters for Zn, AuGe, Ni and AuZn evaporation processes. Filament current was used only for Zn evaporation, while other depositions were adjusted with a beam current.

Target material	Zn	AuZn	Ni	AuGe
Voltage (kV)	2.6	2.7	2.7	2.7
Filament current (mA)	300	-	-	-
Beam current (mA)	-	100	115	110
Pressure (mbar)	1×10^{-6}	2×10^{-6}	6×10^{-6}	2×10^{-6}
Evaporation rate (nm/s)	0.5	0.2	0.1	0.3

5.3 Spin-on glass films

Spin-on-glass films were used to protect the samples during diffusion annealing. On bare parts of the substrates, SOG prevents the decomposition of gallium arsenide, and on top of Zn film, SOG hinders the evaporation of zinc. Two different spin-on-glass solutions, SOG-1 and SOG-2, were used. SOG-1 was commercially available as Accuglass T12 512B and was acquired from Honeywell. It was used as received according to the instructions from the manufacturer. SOG-2 was a self-made mixture of fumed silica in water/ethanol solution that was prepared with a method based on the studies of Vasara [26].

First, a DI-water/ethanol base solution was prepared. Then, amorphous fumed silica acquired from Alfa Aesar with a surface area of 175–225 m^2/g was dispersed into the base solution that was manually stirred and ultrasonicated. The addition of SiO_2 was done in two parts, since this reduces the total stirring time. Before spin coating, the solution was diluted with ethanol to achieve suitable viscosity. Table 3 represents the mixing ratios of the SOG-2 solution that was spin coated.

Table 3: Composition of self-made SOG-2 spin-on-glass solution after diluting to suitable viscosity.

Material	Amount
Ethanol	50.0 ml
DI-water	10.0 ml
Fumed silica	3.5 g

Both SOGs were applied on top of GaAs substrates with Laurell spin coater, model WS-650MZ-23NPP. Due to the very small size of the samples, SOG had to be applied at zero RPM. After SOG application, the spinner was started and used for 20 s at 3000 RPM under normal atmospheric pressure and room temperature.

Three-step baking of the SOG films was carried out to provide gradual solvent evaporation. First, the samples were put on a 80 °C hotplate for one minute. Next, the temperature of the hotplate was increased to 150 °C, and as the set temperature was reached samples were annealed for 1 min. Then, temperature was increased to 250 °C and samples were annealed for another minute. Finally, specimens were removed from the hotplate and cooled down to room temperature in air.

The final cure of the SOG was done in a Thermolyne furnace type FB1300 small benchtop muffle furnace that was controlled with Eurotherm 3216 controller. Cure process was performed at 450 °C for 30 minutes in normal atmospheric pressure. Samples were inserted in the furnace before heating was started, and the heating rate was limited to 30 °C/min to decrease the possibility of thermal shocks which could lead to the cracking of the SOG film [74, 112]. Additionally, samples were annealed in pairs so that their SOG protected surfaces faced each other. This was proved to be an effective way to decrease surface damages of the samples by Vasara [26].

5.4 Diffusion annealing

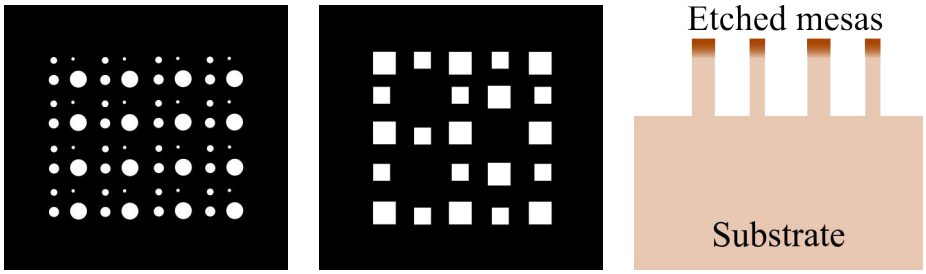
Diffusion annealing was combined to the curing process of the SOG film, and was done directly after the completion of curing in the same furnace. This was done in order to further prevent the cracking of the SOG film during possible cool down and re-heating between cure and diffusion annealing. Additionally, there was no need to separate the processes and extend the total processing and annealing time.

Annealing time of two hours and temperatures between 550 °C and 650 °C were used to perform the Zn diffusion. Annealing was performed in normal air atmosphere using the same protective measures that were used during the cure process. The same heating rate limit of 30 °C/min was used when the temperature was increased from the curing temperature to the diffusion annealing temperature. When specimens were annealed at the desired temperature for two hours, heating elements of the furnace were switched off and samples were cooled down to room temperature inside the furnace. This should help to avoid possible problems caused by rapid and large temperature changes.

After diffusion, samples were removed from the steel container and the Al foil, and cleaned in hydrofluoric and hydrochloric acids. The SOG film was removed by etching in a HF (2.5 M) solution for one minute. Next, the remaining Zn was removed by etching in a HCl (12.0 M) solution for 20 seconds. Samples were thoroughly rinsed in DI water between etching steps and after HCl cleaning. Finally, specimens were dried with nitrogen gas.

5.5 Mesa etching

Small vertical p-n diodes were fabricated on the samples by etching mesa structures on the sample surface. Photo-masks for lithography were printed with a Canon C2225i laser printer on a 3M PP2500 transparency. Fig. 30 represents two mask designs that were used. The initial mask shown in Fig. 30(a) had circular openings with radii of 100, 200, 300 and 500 μm. Later, a more refined mask design illustrated in Fig. 30(b) with larger square openings with side lengths of 1000 and 1400 μm was used.



(a) (b) (c)

Figure 30: (a) The initial photo-mask design with opening radii of 100, 200, 300 and 500 μm. (b) A more adequate photo-mask design with square openings having side lengths of 1000 and 1400 μm. Additionally, an empty space for n-contacts was left in the mask design. (c) Schematic cross-section of the etched mesa structure.

Photosensitive self sticking negative photo-resist tape (INSMA PCB Dry Film 38um) was next applied on the samples. The specimens were heated for 15 seconds at 80 °C to enhance the adhesion between the sample surface and the photo-resist. Next, photo-mask was placed on the sample and a glass piece was put on top of them to keep everything in place. Samples were exposed to room light for 30–60 minutes, so that the illuminated photo-resist becomes insoluble to a resist developer. Exposed samples were developed for 30–45 seconds in a diluted NaOH solution, that dissolved the unexposed areas of the photo-resist film.

Samples with patterned photo-resist were etched in a mixture of citric acid (5.0 M), H_2O_2 (10.0 M) and DI-water with a volumetric ratio of 4:1:4. This solution etched both GaAs and GaAs/AlGaAs DHJ substrates with a rate of 215–250 nm/min. Etching time of 20 minutes was used, to etch through the p-doped surface region of the specimens. This produces mesa structures with a height of 4.3–5.0 μm that

was considered to be more than the junction depth achieved with the Zn diffusion doping. The produced vertical p-n junctions are illustrated in Fig. 30(c). Remaining photo-resist were removed with acetone and a short ultrasonication.

5.6 Metallization

Electrical contacts with good ohmic properties and low resistivity were needed for reliable characterization of the samples. Most of the contacts were elemental indium pieces pressed on the sample surface that were then annealed for 2 minutes at 300 °C on a hotplate in normal room air.

More sophisticated Ni/AuGe contacts for n-type surfaces and AuZn/Zn/AuZn contacts for p-type surfaces were also used. Metals for the contacts were deposited through shadow masks with the evaporation process described in Subsection 5.2. P-type contacts were annealed at 400 °C for 5 min under N_2 flow with a Minibrute quartz tube furnace. N-type contacts were annealed with a Foton 6 RTA system at 450 °C for 15 s under N_2 flow.

5.7 Characterization

Samples were characterized with several different methods including current-voltage (IV) and Hall effect measurements that were used to study the current-voltage characteristics, doping profile and carrier mobility of the samples. In addition, specimens were imaged using scanning electron microscopy and an optical profilometer. A combination of these techniques provides extensive understanding about the samples and the doping process.

5.7.1 IVL measurements

Current-voltage measurement is a tool for analyzing the resistance and resistivity of the semiconductor devices that can be used to estimate internal processes and performance of the devices. For the purpose of this work, IV measurement can also be used to estimate if the Zn diffusion has been successful to form a p-n junction at the surface of n-doped substrates. Successfully formed p-n diode should be clearly visible in the current-voltage characteristics of the device.

In the simplest IV measurement scenario the voltage between two probes is measured while a current is applied across them. However, this method includes extraneous sources of resistance caused by the probe contacts. A more sophisticated way, which minimizes these effects, is to use a 4 point probe measurement illustrated in Fig. 31(a). Here, the voltage is measured between the inner probes and the current is applied across outer ones. This gives more reliable results since separating current and voltage probes eliminates the lead and contact resistances from the measurements.

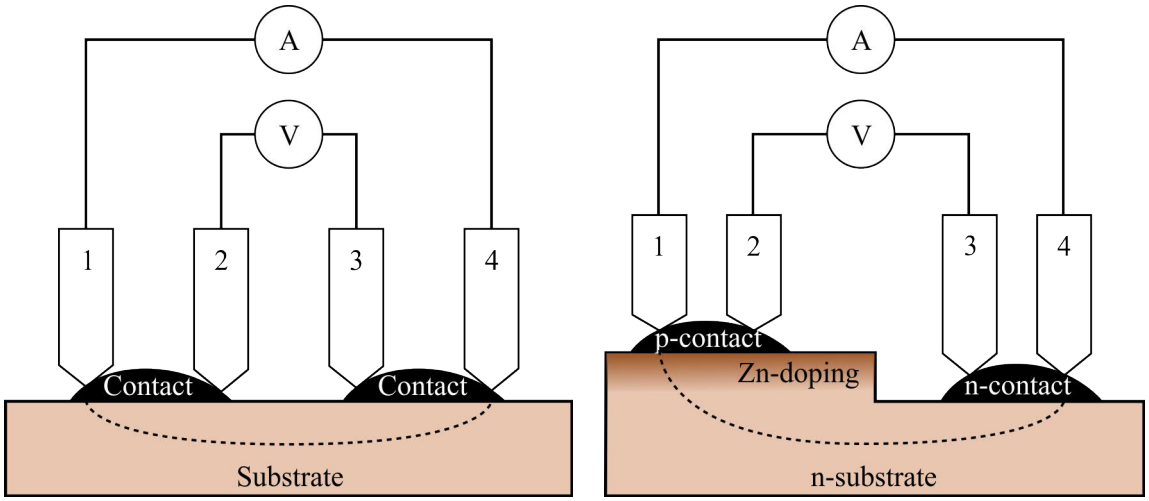


Figure 31: (a) Typical measurement set-up for the 4-point-probe. (b) The set-up that was used in this work. Current is applied between probes 1 and 4 while the voltage between probes 2 and 3 is measured.

In this work, IV measurements performed in the dark were used to analyze the etched vertical p-n diodes. For this purpose p-contacts were fabricated on top of the diodes while n-contacts were placed on the etched surface between the mesas. Fig. 31(b) illustrates the used 4-point-probe setup where two of the probes were placed on the p-contact and other two on n-contact. Normal IV measurements were performed with a HP 4145A semiconductor parameter analysis tool at room temperature.

For the most promising devices, current-voltage-luminance (IVL) tests were also performed. The light emission intensity (L) was imaged with an unfiltered visible and near infrared range camera (C5-2040-4M GigE) with a silicon sensor. IV characteristics with this test setup were measured with a Keithley 2612B System SourceMeter, with a two probe setup.

5.7.2 Scanning electron microscopy

Sample surfaces and cross-sections were imaged and analyzed with two scanning electron microscopes (SEM). A Hitachi tabletop microscope TM-1000 with an energy-dispersive x-ray spectroscopy (EDX) analyzer was used to image the samples and to study the chemical composition of the specimens. A Zeiss Supra 40 was used for higher-resolution SEM images.

In EDX, electron vacancies are formed when the e-beam knocks out some of the inner shell electrons of the sample atoms. As these vacancies are filled by electrons from higher shells, x-rays are emitted with an energy equal to the difference in energy between the shells involved in the electron transitions. Since the electronic structure of each atom is unique, these characteristic x-rays can be used to detect different elements in the specimen. [113].

Due to the interaction volume of the incident electron beam, EDX cannot be used to analyze the topmost surface layer. Depending on the acceleration voltage of the e-beam and the studied material, the characteristic x-rays are generally emitted from the depth of several microns. Furthermore, the detection limit of EDX is limited to a few percents meaning that the doping concentration of Zn cannot be reliably determined with the method. Additionally, detection of light elements (Z<11), such as oxygen, provides typically unreliable results. [113]

5.7.3 Optical profilometry

An optical profilometer was used to visualize etched mesa structures, and determine the etching rate of the etching solution. Profilm3D optical profilometer from Filmetrics was used for the studies. The device was operated in vertical scanning interferometry (VSI) mode that is capable of detecting height differences from 50 nm to 10 mm.

VSI mode uses white light and movement perpendicular to the specimen surface to determine the topography of the sample surface. The incident light from the source is split so that half of it is sent to the sample surface and the other half to a reference mirror. As the light sent to the specimen is reflected and collected, it is combined with the light from the reference mirror. Depending on the surface topography a phase difference between the light beams is detected. This is then analyzed and converted to a height profile of the sample surface.

6 Results and discussion

Results and discussion about the findings of this thesis are presented here, starting from the simulations in Subsection 6.1 followed by the experiments in Subsection 6.2. First, the simulations of the reference device with 6 μm wide structure are presented, and then the effects of increasing the total device width are studied to better understand the general behavior of the DDCT. After the simulation part, experimental results studying the feasibility of lateral doping by diffusion are presented starting with the doping process. Then the results are shown for mesa etching and device contacting. Finally, the IV- and IVL-measurements, and observed light-emission from the vertical p-n diodes are presented.

6.1 Simulations

Simulations were started with the reference device with 6 μm wide structure presented in Subsection 4.1 and Fig. 27, presenting a device that should still be possible to fabricate with optical lithography. Fig. 32 shows (a) the LED current density (defined in Subsection 4.5) and (b) the internal quantum efficiency as a function of bias for the reference structure. The IV curve shows clearly two regimes with different ideality factors (m) that were extracted with Eq. (18). Ideality factor of 1.9 was obtained at low biases (< 0.85 V) and 1.0 at higher biases (> 0.85 V). These values correspond well to the theoretical model of a real diode [37] where SRH recombination dominates at low biases with $m = 2.0$, and radiative recombination with $m = 1.0$ dominates at higher biases. This indicates that the radiative recombination starts to dominate in the reference structure already at biases higher than 0.85 V.

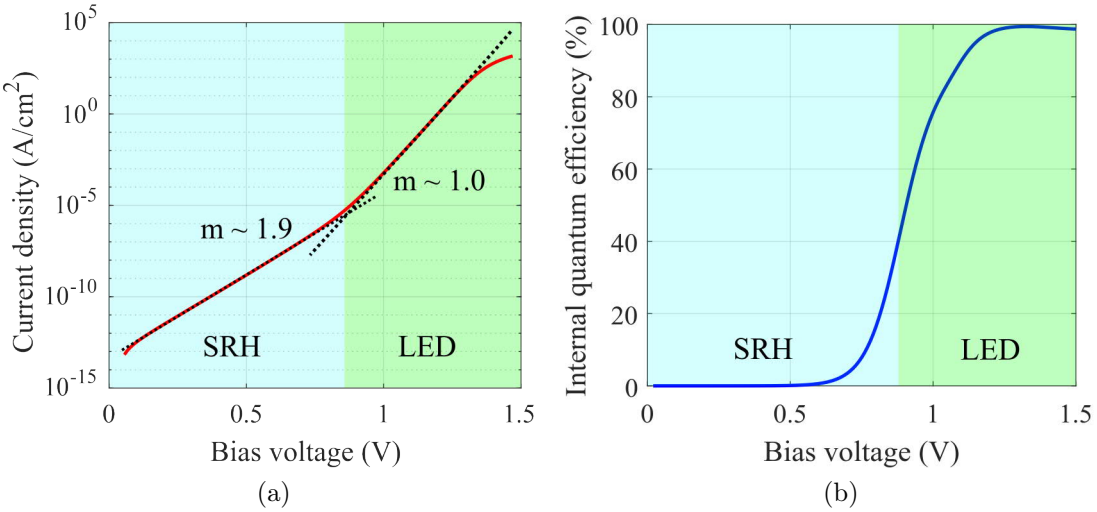


Figure 32: (a) The IV curve of the 6 μm wide reference structure (Fig. 27) showing two regimes for the device operation. At low biases, recombination occurs via SRH recombination and at higher biases radiative recombination dominates. (b) The IQE of the structure, as a function of bias, starts to increase as recombination shifts from SRH to radiative recombination, and stays over 98.0 % at biases of 1.2–1.5 V.

Fig. 32(b) illustrates the internal quantum efficiency of the reference structure showing a peak IQE of 99.4% at a bias of ∼1.33 V corresponding to a current density of ∼100 A/cm^2. Additionally, it is observed that the IQE stays over 98 % for a wide range of biases between 1.2 V and 1.5 V. This clearly shows, that from the modeling point of view, the proposed DDCT structure performs extremely well, and is not substantially degraded by leakage currents or other similar effects that might be more pronounced in the new device structure. Additionally, the achieved IQE values are very close to the experimental values obtained for optically pumped vertical GaAs/AlGaAs DHJ structures by Schnitzer *et al.* [114] who achieved an IQE of 99.7 %, showing that the presence of a p-n junction does not practically affect the achievable IQE of the structure. In part due to the better general quality of GaAs materials, the IQE of our structure is also significantly higher compared to high-efficiency GaN structures [7] with IQE of roughly 85 % at similar current densities. At such high currents, the efficiency of GaN LED is also limited by the efficiency droop resulting from Auger recombination and leakage mechanisms

Fig. 33 illustrates a) the radiative and total recombination rates and b) charge carrier concentrations as a function of lateral position within the active region of the LED. Two observations are made from Fig. 33(a). Firstly, by comparing the radiative and total recombination rates, it is noted that the IQE within the AR is very high at all positions. Secondly, the recombination rate is higher under the p-contact, as compared to the n-contact side. The non-uniformity of the recombination rate is explained mostly with the lower hole concentration under the n-type contact as observed in Fig. 33(b). This observation is explained by the lower mobility of holes in GaAs and AlGaAs.

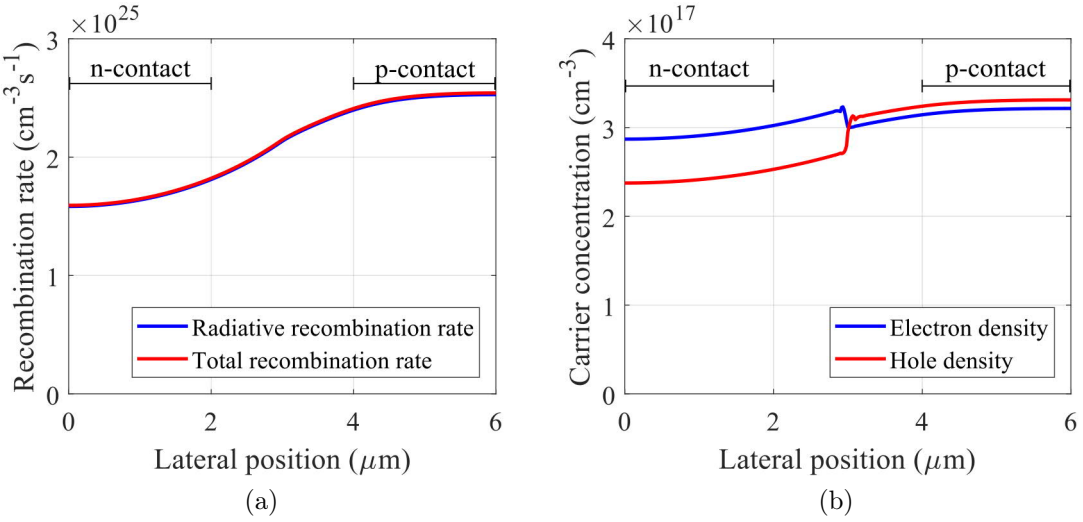


Figure 33: (a) Radiative and total recombination rates within the active region as a function of lateral position showing slightly stronger recombination under the p-contact at ∼100 A/cm^2. (b) Carrier concentrations within the AR as a function of lateral position at ∼100 A/cm^2 indicates that the recombination rate is limited by the concentration of holes under the n-contact area.

Additionally, Fig. 33(b) shows an abrupt change in carrier concentrations at the middle of the structure, that is related to the modulation doping [115] due to the lateral p-n junction located directly above the AR in the AlGaAs layer. As the presence of the p-n junction can be observed in the AR, it is concluded that holes are effectively spread across the whole p-region. A similar behavior is present also for electrons, but the change is smaller compared to holes. Furthermore, the electron concentration reduces under the n-contact as the lateral position approaches zero, which might be explained by the bending of the hole quasi-Fermi level illustrated later. These findings are very interesting and since their nature is not fully understood at the time, further investigations should be done in the future.

Fig. 34 shows the 2D distribution of the total recombination rate at ∼100 A/cm^2 in the reference structure clearly showing that practically all of the recombination is confined within the active layer. Additionally, it is confirmed that the recombination rate in AR does not depend on the y-position. This finding highlights the efficiency of the injection method as holes can clearly reach the bottom of the active layer.

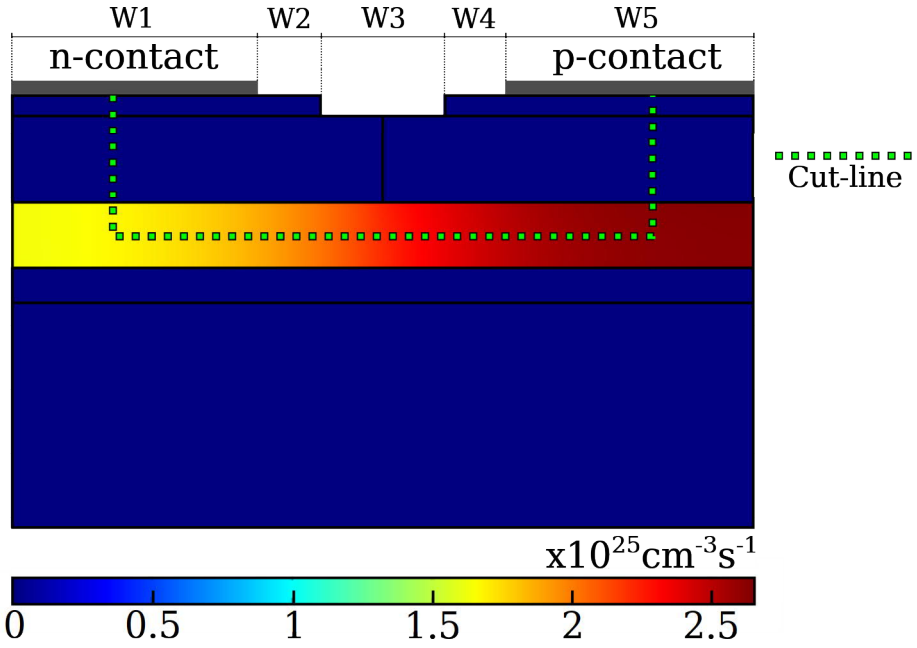


Figure 34: 2D map of the total recombination rate at 100 A/cm^2 in the 6 μm reference structure showing that recombination is completely confined within the active region. Additionally, a cut-line to be used for band diagrams in Fig. 35 is shown.

Fig. 35 shows the band diagram of the reference structure at 100 A/cm^2 following the cut-line illustrated in Fig. 34. Electrons are injected from the left side contact and holes from the right side contact. It can be seen that both charge carrier can enter active region with a relatively low potential barrier, but are still strongly confined by the AlGaAs barriers on the opposite side of the diagram. After closer inspections of these barriers, it was observed that the barriers do not cause any significant quasi-Fermi losses.

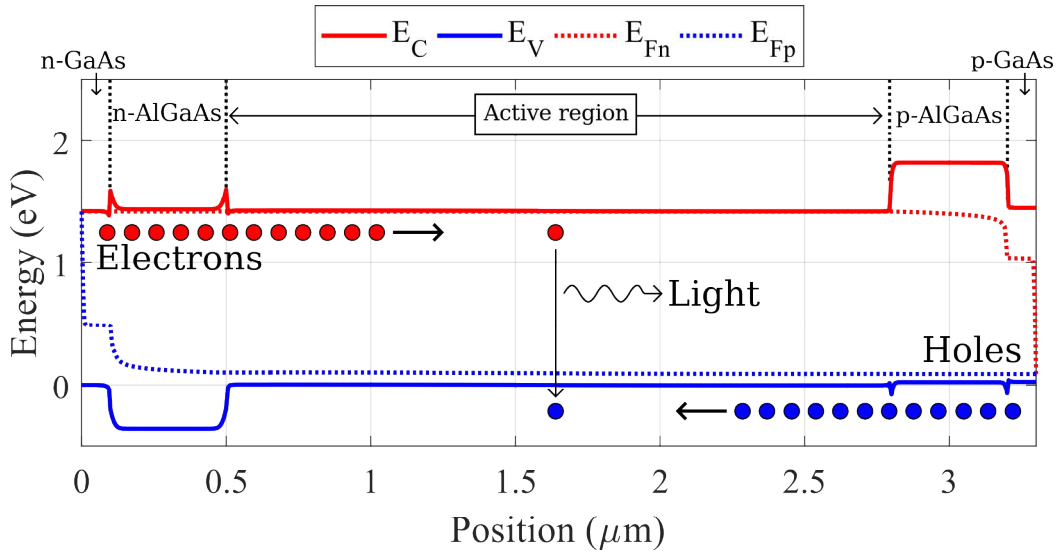


Figure 35: Band diagram of the reference structure following the cut-line defined in Fig. 34. Electrons from the left and holes from the right can enter the AR with small barriers. E_C corresponds to the conduction band edge, E_V to the valence band edge, E_{Fn} to the quasi-Fermi level for electrons, and E_{Fp} to the quasi-Fermi level for holes.

The width of the LED was scaled gradually to 30 μm to see how the profile of the net recombination and other device properties change. Fig. 36 shows the radiative recombination rate as a function of a relative position in the x-direction, where the total width of each device is normalized for easier comparison between the structures. As the total width increases, the recombination focuses more at the p-contact, as expected due to the low mobility of holes. More interestingly, no signs of current

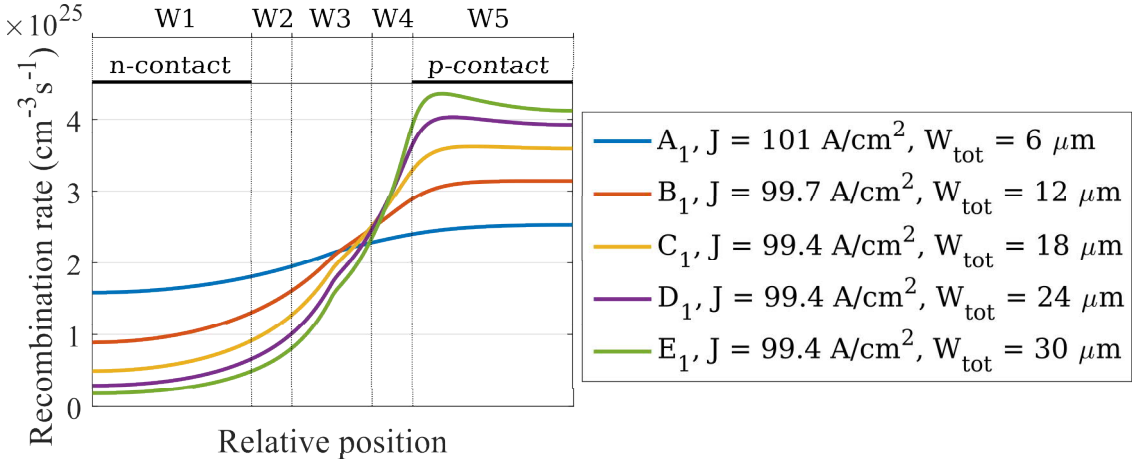


Figure 36: Radiative recombination rate within the AR as a function of relative position for structures A, B, C, D and E with normalized widths. As the total width (W_{tot}) of the device increases, the uniformity of the recombination decreases as it concentrates under the p-contact. The annotations W1 - W5 denote the widths of different parts of the devices shown in Table 4.

crowding at contact edges is observed for structures A, B and C. However, structure D and especially E, show some signs of possible current crowding, as the highest recombination rate is more focused at the p-contact edge.

Table 4 provides a more detailed description of the wider structures and some of their key figures of merit. From this data, it can be observed that the required bias for reaching a current density of 100 A/cm^2 increases slightly as the total width is increased. Additionally, a significant increase in the amount of radiative recombination under the p-contact is noticed as the width is increased.

Table 4: Detailed performance and lateral dimensions of the simulated structures at a current density of approximately 100 A/cm^2 for five different device widths ranging from 6 μm (A) to 30 μm (E). Reduced uniformity for the radiative recombination (*determined with Eq. 40) can be observed as the total width of the device is increased.

Structure	A	B	C	D	E
Bias (V)	1.329	1.336	1.342	1.348	1.354
Current density (A/cm^2)	101	99.7	98.9	99.4	99.4
IQE (%)	99.4	99.4	99.4	99.4	99.4
Uniformity* (%)	**62.6**	**28.3**	**13.6**	**7.15**	**4.11**
W$_{\mathrm{tot}}$ (μm)	**6.0**	**12**	**18**	**24**	**30**
W1 = n-contact (μm)	2.0	4.0	6.0	8.0	10.0
W2 (μm)	0.5	1.0	1.5	2.0	2.5
W3 (μm)	1.0	2.0	3.0	4.0	5.0
W4 (μm)	0.5	1.0	1.5	2.0	2.5
W5 = p-contact (μm)	2.0	4.0	6.0	8.0	10.0

A few preliminary tests were done to enhance the uniformity of the recombination in the larger structures. As the low mobility of holes is likely the main reason for the focused recombination under the p-region, a p-doped (3×10^{17} cm^{-3}) substrate and a p-AlGaAs barrier layer under the AR were tested. This should introduce additional modulation doping for holes that increases the amount of holes available for current transport in the active region. Fig. 37 illustrates a significant change in uniformity of the recombination rate for the 12 μm wide structures. The uniformity was increased from 28.3 % for n-doped bottom layers to 49.0 % for p-doped layers. The introduction of hole modulation doping lead also to a change in the carrier concentrations as the average hole density in AR was increased by 8.9 % and the electron density reduced by 5.9 %. This effectively balances the carrier concentration under the n-contact and increases the uniformity of the recombination.

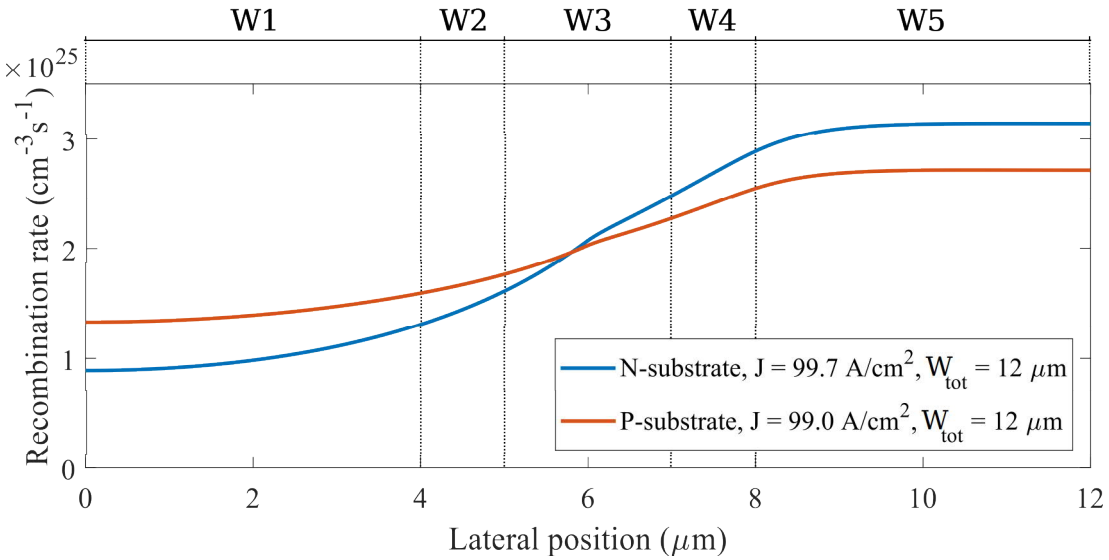


Figure 37: Radiative recombination rate as a function of lateral position for the 12 μm structure showing a significant enhancement in the uniformity as the doping type of the substrate and the AlGaAs barrier layer under the AR is changed from n to p.

Overall, the simulations have shown that the proposed GaAs/AlGaAs DHJ DDCT LED structure can provide very high internal quantum efficiencies at high current injection. Similar results have been recently obtained also for GaN based DDCT LEDs in our group [15, 16]. These results can be promising also for thermophotonic cooling applications such as the thermophotonic heat pump [18] and double-diode structures [19, 21]. Even with these encouraging results, there are still several features to be optimized. For example, improvements could be achieved by changing the doping type of the substrate and AlGaAs barrier layer below the AR, as indicated by the results of this work. Additionally, the lateral dimensions and geometry should be optimized in the future to maximize the device performance.

It is noteworthy that the presented simulations are part of a preliminary study of the DDCT efficiency. For example, surface recombination processes were excluded from the model used here. Since the structure was proven to be highly efficient at high injection currents, it is clear that further investigations on the structure are in order. In future work, the simulation parameters should be calibrated with the measurement results, the missing recombination processes should be included in the model and the model should be extended to allow estimations of the external quantum efficiency and wall-plug efficiency. As the results indicated, the smallest lateral dimensions provided the best performance and the most uniform recombination within the active region. Repeating this unit to form a multi-finger structure could enable large-area LEDs with highly uniform recombination profiles. Also, optimizing the device geometry to account for the differences in carrier mobilities e.g. by using asymmetric p- and n-contact widths could provide means to further improve the excitation uniformity well within the limits of optical lithography.

6.2 Experiments

In total, this thesis included 30 different experiments with varying thermal annealing and sample protection parameters to study the Zn diffusion into the substrates described in Section 5. The most successful experimental samples, for which the results were analyzed, are described in Table 5. Sample HJ1 was the first p-n homojunction specimen showing signs of a p-n junction, and it was used mainly to characterize the Zn doping. Specimens HJ2–HJ4 were the most successful homojunction samples fabricated on n-GaAs substrates, and DHJ1–DHJ3 were the most successful specimens fabricated on GaAs/AlGaAs double heterojunction substrates. In addition to this, some of the unsuccessful diffusion doping attempts are discussed.

Table 5: Details of the substrates, main parameters of the diffusion doping process and thicknesses of the dopant source films for the most important diffusion doped samples that were fabricated and analyzed during the research. Samples HJ1–HJ4 are referring to the doped n-GaAs substrates and DHJ1–DHJ3 to the MOVPE grown GaAs/AlGaAs double heterojunction samples. Diffusion annealings of the specimens were performed without protective atmosphere in normal room air.

Sample	Substrate	Substrate n-doping	Diffusion process	Zn film
HJ1	GaAs	1×10^{18} cm^{-3}	2 h, 650 °C	400 nm
HJ2	GaAs	2×10^{18} cm^{-3}	2 h, 550 °C	400 nm
HJ3	GaAs	2×10^{18} cm^{-3}	2 h, 600 °C	400 nm
HJ4	GaAs	2×10^{18} cm^{-3}	2 h, 650 °C	400 nm
DHJ1	GaAs/AlGaAs	3×10^{17} cm^{-3}	2 h, 550 °C	400 nm
DHJ2	GaAs/AlGaAs	3×10^{17} cm^{-3}	2 h, 600 °C	400 nm
DHJ3	GaAs/AlGaAs	3×10^{17} cm^{-3}	2 h, 650 °C	400 nm

6.2.1 Diffusion doping

Fig. 38 illustrates an SEM cross-section from the middle of sample HJ1 after cleaning with HF and HCl, showing clearly a brighter layer on the surface of the sample. Several similarities can be found between Fig. 38 and the results from Perovic *et al.* [116] who observed similar contrast differences between bright p-doped and darker n-doped GaAs layers with almost identical dopant concentrations. This indicates that the bright layer in Fig. 38 is in fact a p-GaAs layer with an approximate thickness of 1.8 μm. Based on the results of Ye *et al.* [47] and Lawrence *et al.* [63], this kind of junction depth or even deeper is achievable in two hours. An additional observation made from Fig. 38 is that the interface between n- and p-GaAs is very clear, although this is expected from the sharp diffusion front that is usually observed for Zn diffusion as discussed in Subsection 2.3.2.

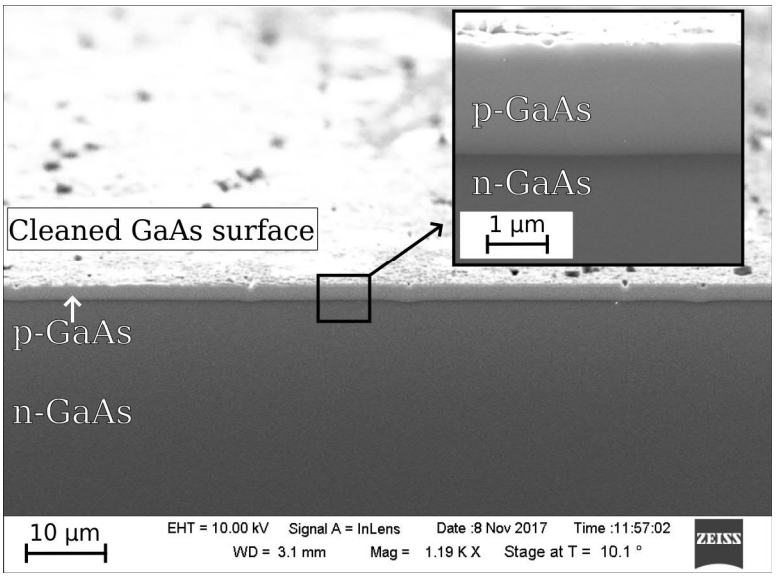


Figure 38: Cross-section SEM image of sample HJ1 showing a ∼1.8 μm deep diffusion doped area in the surface region of the n-GaAs substrate. The sample was tilted by 10.1°, also making the cleaned surface visible.

Based on the SEM cross-sections, the protective SOG film and other measures were able to successfully protect the middle of the sample allowing uniform Zn doping. However, the junction depth decreased away from the center indicating that the protection was not equally successful at the edges of the Zn coated area. This might be a result of the diffusion doping setup where processed sample surfaces were facing each other. It is possible that at the edges of the sample, SOG and Zn films can evaporate and escape the minimal space left between the surfaces. At the middle of the sample, the evaporated atoms cannot escape the gap between surfaces which seems to hinder the decomposition of the sample. Furthermore, it is possible that the Zn film thickness has been uneven.

Fig. 39 presents more detailed SEM images of the cleaned surface of HJ1, showing a significant change between Fig. 39(a) and Fig. 39(b) where Zn was not deposited under the SOG film, and Fig. 39(c) and Fig. 39(d) where Zn film was deposited, indicating that the extensive surface roughness is clearly related to the presence of the Zn film. The actual mechanism leading to roughening is not known at the time, although several possibilities have been identified. The first explanation is that the diffusion of zinc atoms could lead to surface roughening. However, Sakai *et al.* [72] reported mirror like surfaces with very similar diffusion doping process by using a ZnO film as a dopant source, though it is possible that the higher thermal stability of ZnO compared to elemental Zn provided better substrate surface quality. The second possibility is that the presence of oxygen during the doping process leads to oxidation of the materials, but this would be in conflict with the observation that SOG protects the surface areas without Zn, as seen in Fig. 39(a) and Fig. 39(b). The third option is that some chemical reactions occur between the Zn film and the GaAs substrate surface. Lawrence *et al.* [63] found out that a reaction between CVD deposited $(ZnO)_x(SiO_2)_{1-x}$ dopant source and a GaAs substrate formed $ZnGa_2O_4$

spinel phase that consumed some of the GaAs and caused the surface roughening. Additionally some Zn precipitates might have been formed due to the very high Zn surface concentration caused by the Zn thin film.

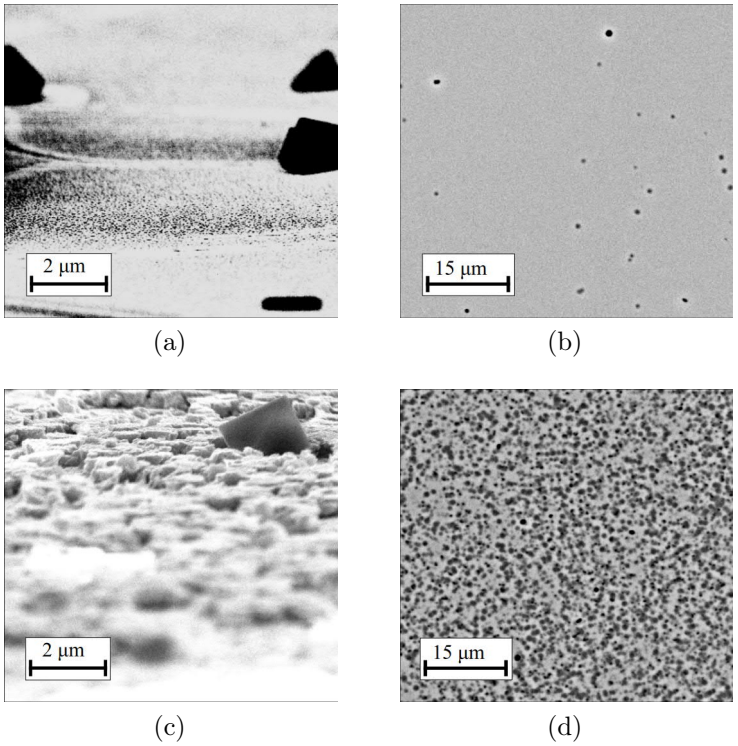


Figure 39: SEM images of the cleaned surface of HJ1 showing a very significant difference between Figs. (a) and (b) with the surface covered only by SOG during the annealing, and Figs. (c) and (d) where Zn was deposited below the SOG. Figs. (a) and (c) are cross-section images where samples were tilted by 10.1°, and Figs. (b) and (d) are normal SEM images.

Generally, somewhat rough surfaces were observed for all of the samples, but the extent of surface damage varied greatly. A significant amount of the diffusion attempts were unsuccessful due to a huge amount of surface damage in the areas where the Zn film was deposited. A clear reason for the variance of the surface quality could not be identified during the studies.

For most samples, a 400 nm thick Zn film was used as the dopant source. Compared to the work of Goldstein [71] who used electroplated zinc film as a dopant source, the amount of Zn is in the same range. On the other hand, Sakai *et al.* [72] used 50 nm thick ZnO films which is much lower. Some test were also carried out with thinner films using thicknesses of 20, 50 and 200 nm. Based on these few tests, 20 and 50 nm of zinc were not enough for a successful fabrication of a p-n junction. SEM images and chemical analysis with EDX indicated that during diffusion annealing, a significant part of the Zn diffused to the undoped SOG film protecting the surface. Consequently, there was not enough Zn diffusing into the substrate. Additionally, the quality of thinner Zn films was found to be much lower.

Zn film was chosen as the dopant source due to the relative simplicity of the doping process from solid sources and a high Zn surface concentration provided with the film. In addition, doping from vapor phase and ion implantation could not be used in this work due to possible Zn cross contamination problems at Micronova facilities. As mentioned above, the Zn film is definitely related to the surface roughening, and it could also explain the uneven doping depth between sample center and edges of the Zn coated area. One disadvantage of the solid Zn source is its melting point of 419.13 °C, which is much lower than the temperatures required for diffusion doping. Furthermore, the evaporation process for Zn deposition was quite difficult to control due to the high vapor pressure of zinc.

As discussed in Subsection 2.2.3, protective measures play a crucial role in preventing the thermal decomposition of GaAs substrates and other III-V materials. In this work, the main protective method was the SOG film that was spin-coated on the substrate surface. In optimal case Zn diffusion annealing should be done in a protective atmosphere to prevent the oxidation and the desorption of unprotected GaAs substrate. During this work, a furnace with controllable atmosphere was not available for the diffusion process, due to the risks of Zn cross contamination. A compromise solution was to use steel container and Al foil around the GaAs specimens, to minimize the reactions between GaAs and oxygen. This was by no mean an ideal solution for the problem, but with SOG, zinc was successfully diffused into the samples.

Just before the end of this work, we had a chance to test the diffusion process inside a glow box with nitrogen atmosphere, by placing the whole furnace inside the box. There was time for only a single diffusion doping test that was performed at 600 °C for 2 hours. Based on visual inspections, removing the oxygen from the process made a huge difference for the surface quality of the substrates and the protective SOG film. However, the normal cleaning process with HF and HCl was not able to remove all of the films on the sample surface. Several different solutions were tested without success and a working cleaning process that would preserve the GaAs substrate was not found in time. These findings indicate that some unexpected chemical reactions might occur when the oxygen is removed from the process. Unfortunately, there was no time to properly analyze these samples or the nonremoved film. Anyway, diffusion in N_2 atmosphere gave very promising results as the surface quality in successfully cleaned areas seemed to be very good, indicating that the possible future work with the doping process should be continued with the protective atmosphere.

Hall measurements were planned to determine the carrier concentration of the p-doped layer, but unfortunately, the measurement setup was out-of-use for most of the time. The tool was fixed during the final stages this thesis, but no suitable samples were available for the analysis at that time. Older successfully doped specimens were already processed into mesa structures. Additionally, characterizing of p-doped region on the surface of an n-GaAs substrate could have compromised the reliability of the results due to the high electrical conductivity of the substrate that could introduce leakage currents to the Hall measurement results.

Due to the above-mentioned problems, the diffusion of Zn into intrinsic GaAs substrate was also attempted during the last weeks of the work. Three sets of samples for the Hall measurement were prepared but the sample surface quality was extremely bad. No changes for the actual process were made, so it is assumed that the change in the substrate doping is the reason for the problems. Kahen *et al.* [61, 51] observed slower Zn diffusion for n-doped GaAs substrates compared to i-GaAs. This indicates, that if the surface damages observed in the present work are caused by the diffusion of Zn into the substrate, undoped substrates may be more easily damaged with the presently used process.

Based on the SEM cross-sections, no visible macroscopic damage was observed within the p-doped layer which is promising for the possible use of the doping process for realizing the simulated DDCT structures. However, it is possible that microscopic damages that cannot be detected with SEM exist in the samples. Additionally, Ky *et al.* [69] observed that Zn diffusion causes the disordering of the lattice behind the Zn diffusion front. However, in the optimized fabrication of proposed DDCT LEDs, the doped region would not extend to the active region of the LED. This could indicate that the device performance might be mainly unaffected by the damaged p-layer, although the hole mobility and life-time in the p-type region might be affected.

6.2.2 Mesa etching

Fig. 40 shows an image of a square mesa with a side length of ∼1.4 mm and a height of approximately ∼4.2 μm that was obtained with the optical profilometer. This confirmed that the etching process was able to produce vertical p-n diodes with adequate quality despite the simplicity of the lithography process. Additionally, similar imaging was used to estimate the etching rate of the used etching solution that was found to be ∼220 nm/min.

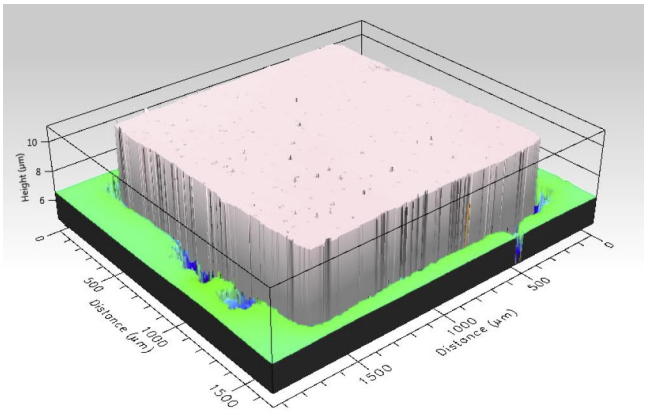


Figure 40: 3D image of the etched mesa with a side length of ∼1.4 mm and a height of ∼4.2 μm. Trenches seen around the mesa were not observed with SEM, indicating that they are artifacts caused by the measurement method, that do not corresponds to the actual topography of the sample.

6.2.3 Metallization

Due to some unexpected results in using indium contacts in the beginning of the experimental studies, a more detailed contact study was performed on the effect of indium annealing time on two n-GaAs substrates with silicon concentrations of 1.5×10^{17} cm^{-3} and 2.0×10^{18} cm^{-3}, and one p-GaAs substrate with a zinc concentration of 1.0×10^{19} cm^{-3}. Fig. 41 illustrates the IV curves of In contacts annealed in varying temperatures, showing that adequately ohmic contacts can be fabricated on all of the substrates if the annealing temperature is 300 °C. Ohmic contacts were also achieved after annealing at 350 °C or higher, although the oxidation of indium begins to cause problems above temperature of 350 °C.

Fig. 41 shows also that the resistance of the contacts decreases with an increasing doping concentration of the substrates. This was expected because increasing the doping concentration narrows the depletion region formed at metal-semiconductor interface, which enables easier tunneling of the charge carriers through the barrier that is formed at the interface. For example, on the p-GaAs substrate with the highest concentration, the contacts were ohmic at all temperatures.

Additionally, the effect of the elevated temperatures used for diffusion doping was tested with n-GaAs substrate. For this test, samples coated only with the protective SOG film were annealed with normal diffusion doped samples. Results of these tests indicated no signs of material degradation caused by the annealing process, as the IV measurements of the samples did not change compared to unprotected substrates. This verifies that most of the problems in the diffusion doping process are caused by the Zn-film.

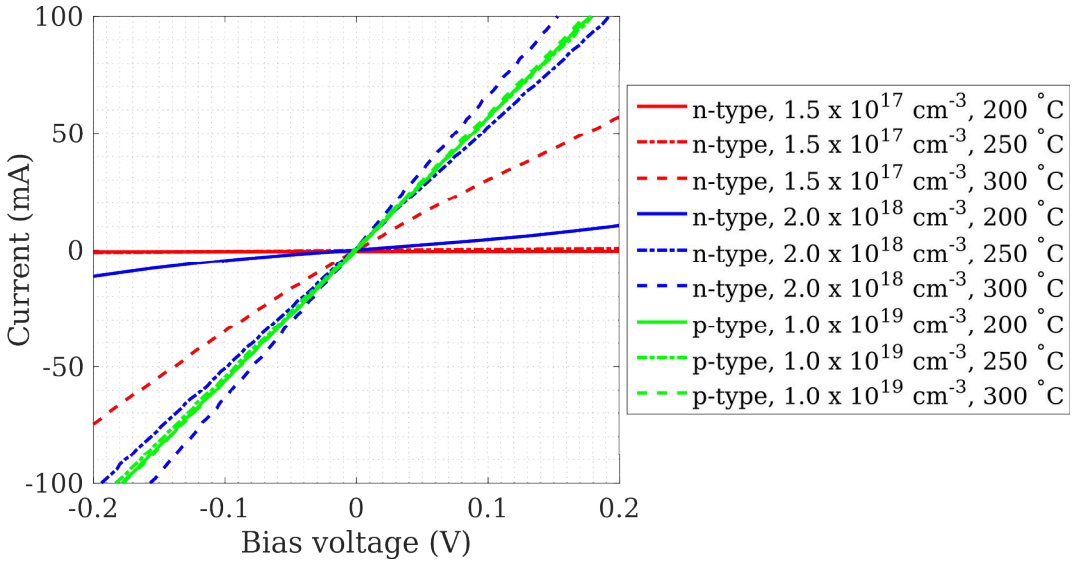


Figure 41: IV-characteristics of the In contacts on various substrates, showing that all contacts are relatively ohmic if they have been annealed at 300 °C, and that the quality of the contacts increases with the doping concentration of the substrate. Annealing time of 2 min was used for all contacts. Green IV curves of the p-contacts were not affected by the annealing temperature, so they are on top of each other.

These results show that indium contacts are suitable for characterizing the fabricated devices. All samples were characterized with In contacts that were annealed for 2 minutes at 300 °C. However, In contacts are mechanically rather weak, susceptible for oxidation, and they have a relatively high contact resistance. Due to these aspects, evaporated AuGe/Ni contacts for n-surfaces and AuZn/Zn/AuZn contacts for p-surfaces should have been used in testing the final structures. Unfortunately, the RTA system and tube furnace that would have been required for the contact annealing were out-of-use during the final stages of the studies.

6.2.4 IV-measurements

Fig. 42 shows the IV measurements of the mesa structures with an area of 1 mm^2 fabricated on samples DHJ1 - DHJ3. All of these mesas showed diode-like behavior. However, quite low threshold voltages were observed for samples DHJ1 and DHJ2 compared to the GaAs band-gap energy of 1.42 eV. Additionally, increasing threshold voltages and decreasing leakage currents are observed for higher diffusion annealing temperatures. A clear reason was not confirmed for this behavior, but a few possible causes for it can be given. One viable explanation for this behavior is that the p-doped region is rather narrow so that indium atoms from the p-contact can partially diffuse through the p-n junction during contact annealing to form conductive channels. Especially, if the p-doped layer is damaged to some extent, the In diffusion might be very fast. As higher temperatures should produce deeper junction depths, the diffusing indium atoms would not be able to diffuse through the p-n junction, which would result in threshold voltages approaching the theoretically expected values. Another possibility could be that the Zn film thickness has been uneven, resulting in a non-uniform doping depth.

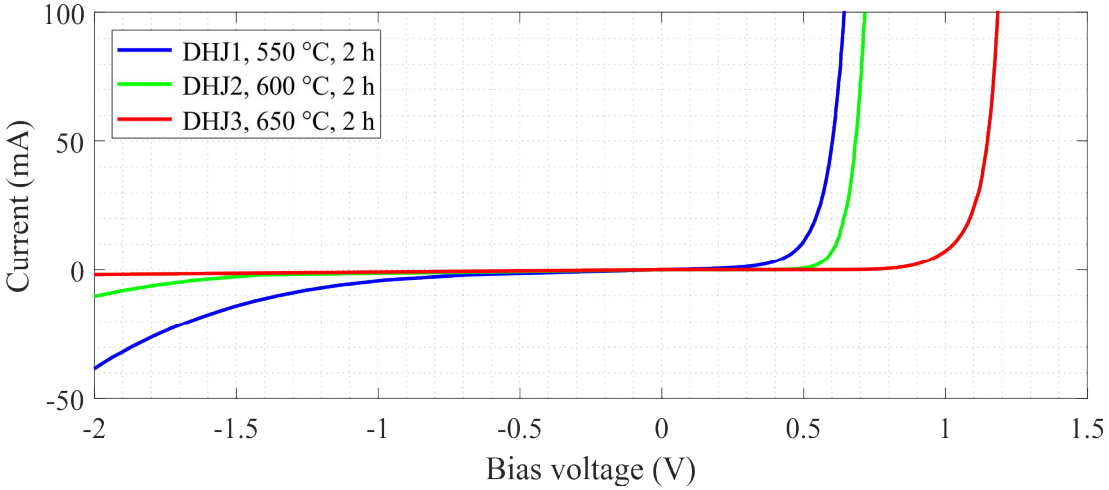


Figure 42: Measured IV curves for GaAs/AlGaAs samples DHJ1–DHJ3 showing that the required threshold voltage under forward bias, where substantial current starts to flow through the diodes, increases with annealing temperature and approximately reaches the theoretically expected level at the highest annealing temperature of 650 °C.

Fig. 43 presents the IV-curve for one of the mesas on sample DHJ3 on a logarithmic scale, showing two separate SRH-like recombination regions with slightly different ideality factors and effective A-parameter values extracted with Eq. 38. Fig. 43 shows that already at approximately 0.87 V, the LED current begins to saturate. According to Schubert [37], this current saturation can be explained by a series resistance. No clear reason for the high resistance has been identified, but it is most likely related to the contact resistance induced by In-contacts and the possible material degradation due to the diffusion of Zn. The latter possibility would agree with the high A-parameter value extracted from the IV data, that is most likely explained with the reduced material quality. Overall, the estimated material parameters are qualitatively in line with the simple diode models discussed in earlier chapters, but gaining more accurate insight into the applicable device physics will also require more quantitative further comparisons.

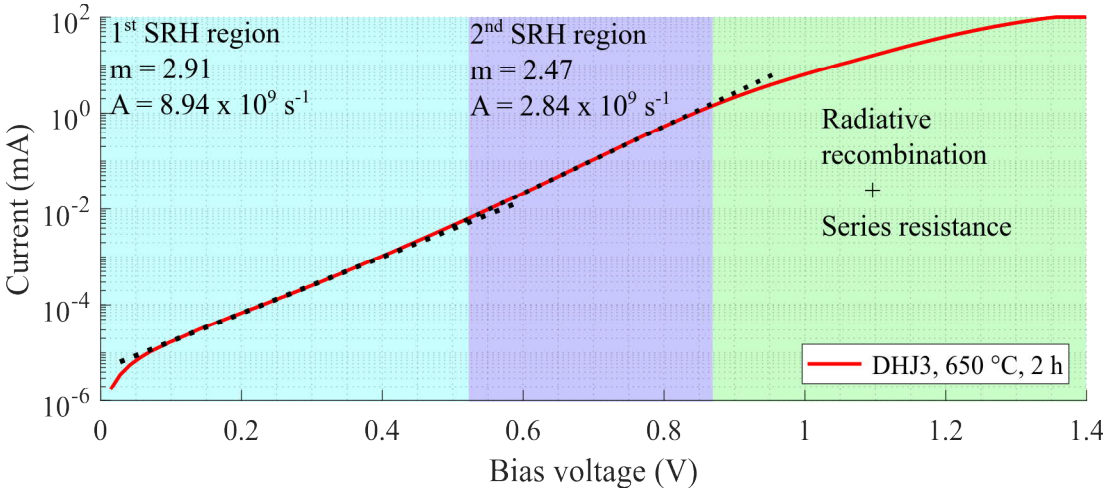


Figure 43: IV curve of DHJ3 on a logarithmic y-axis showing two SRH dominated regions with slightly different properties. Additionally, a series resistance is observed above a bias voltage of 0.87 V.

Fig. 44 represents results for similar IV measurements for 1 mm^2 diodes fabricated on samples HJ2–HJ4, showing generally much worse IV-characteristics. The variation between samples is higher, and a similar temperature dependence between the diode properties and the annealing temperature could not be identified. For example, highest threshold voltages were observed for HJ3 annealed at 600 °C. However, the shape of the IV curve is quite unusual compared to other curves in Fig. 42 and Fig. 44. The difference between HJ2 and HJ4 is more similar to the GaAs/AlGaAs samples in the Fig. 42, although the threshold voltage is very low and a leakage current is very high for HJ2. Based on these results, the fabricated p-n diodes on GaAs/AlGaAs samples have a higher quality than those fabricated on n-GaAs substrates, but a more reliable evaluation of the effects of the annealing temperature and substrate properties on the device performance will necessitate a more systematic study of an even larger number of samples.

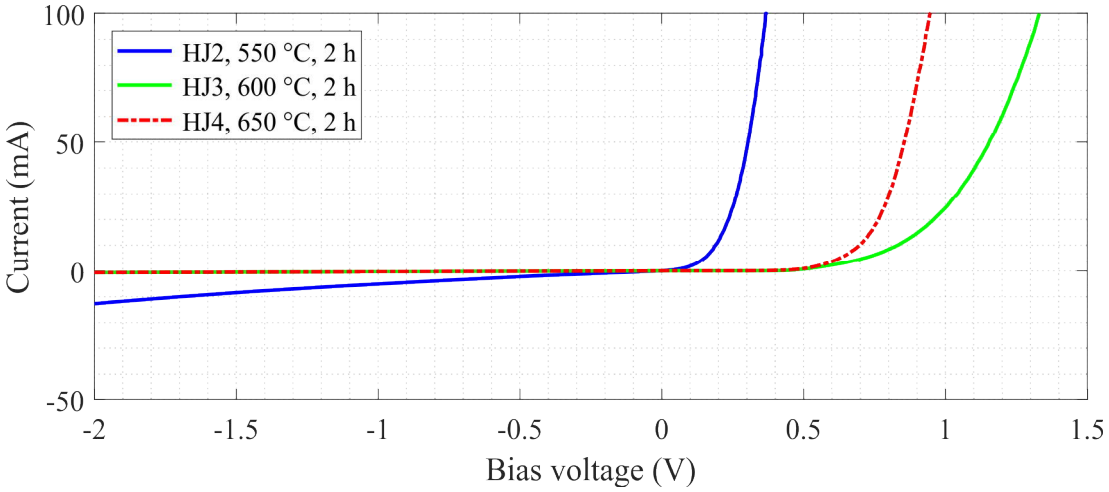


Figure 44: Measured IV curves for GaAs samples HJ2–HJ4. It can be noticed that the required threshold voltage where current starts to flow through the diodes reaches a maximum at an annealing temperature of 600 °C.

6.2.5 Light emission

Fig. 45 shows the light emission distribution at 10, 50 and 100 mA for a 1 mm^2 mesa fabricated on sample DHJ3, whose IV curve was presented in Fig. 43. It can be clearly seen that as the injection current increases, the light emission focuses more strongly under the indium contact. This is expected since a dedicated current-spreading layer was not used, and the sample was not intended for high current densities. Light emission in Fig. 45 was normalized by dividing the intensity of each pixel with the maximum value obtained at 100 mA to produce comparable images.

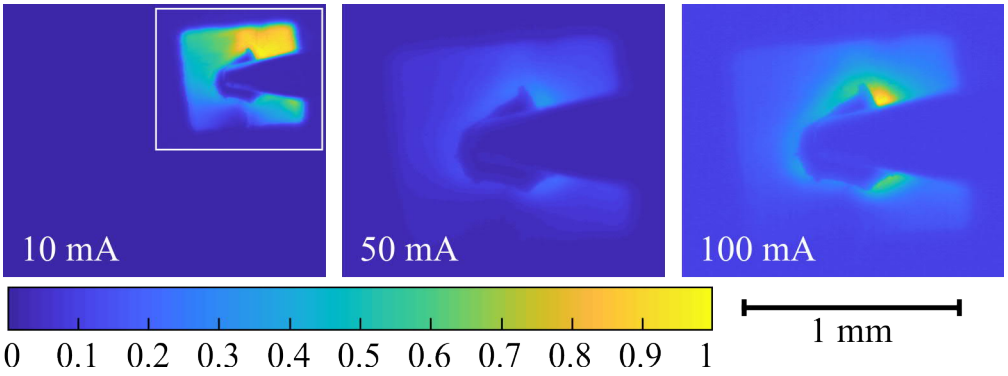


Figure 45: Light emission from sample DHJ3 as measured from one of the vertical LEDs with a surface area of 1 mm^2, and normalized by the maximum value at 100 mA. The inset at 10 mA also illustrates the light emission normalized by the maximum value at 10 mA to show the more uniform current spreading at small currents. At 50 mA, light emission is more strongly focused around the contact, and at 100 mA the strongest light emission is clearly observed at the edges of the In contact indicating that almost all of the recombination occurs under it.

Fig. 46 shows the IV-curve and the measured light emission in arbitrary units in linear (a) and logarithmic (b) scale. It is shown that the light emission exceeds the detection threshold at a bias of approximately 0.85 V. A more detailed inspection of the current vs light emission shown in Fig. 46(b) revealed that the device includes a radiative recombination dominated regime above a bias voltage of ∼1.3 V. Furthermore, at higher biases, some resistive losses can be observed as the current starts to saturate, as was already seen in the plain IV-measurements in Fig. 43.

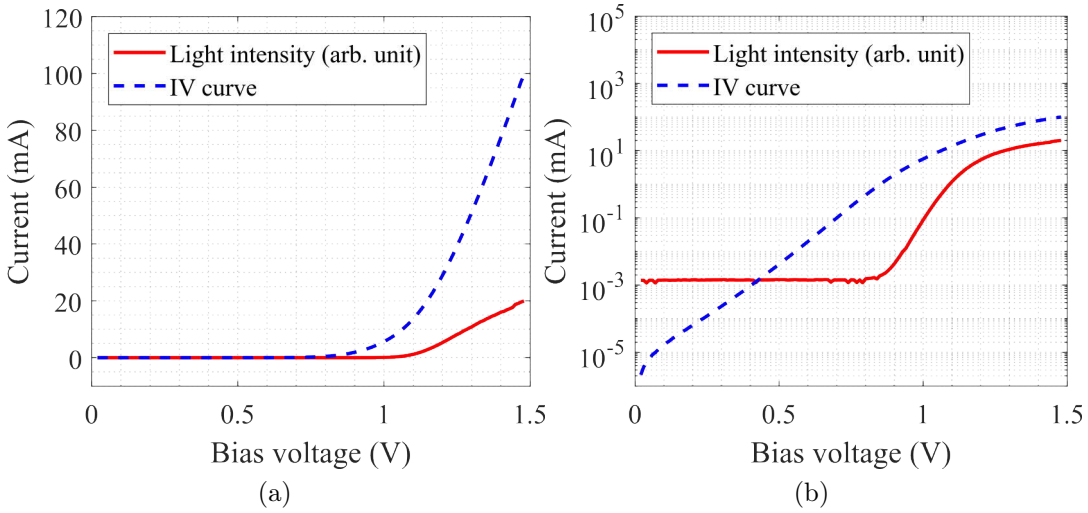


Figure 46: (a) IVL measurement of sample DHJ3 on a linear scale showing that light emission from the sample is clearly observed. (b) IVL curve of sample DHJ3 on a logarithmic y-axis showing that the slope of the light emission curve is approximately twice as large as the slope of the electric current, as expected from the recombination theory. Resistive losses begin to appear at around 0.85 V and a radiative recombination dominated regime was found above a bias voltage of ∼1.3 V.

7 Conclusions

In this work, first simulations of a novel GaAs/AlGaAs DHJ LED based on DDCT current injection scheme were performed in order to explore the general requirements and limitations of the suggested device structure. Also, the viability of the Zn diffusion doping process for realizing the simulated structure was experimentally evaluated.

Simulations indicated that the device design could enable high-efficiency LEDs for large-area applications if an optimized finger structure is used to create a large array of small DDCT units. The simulation results indicated that by fully optimizing the LED design and especially the lateral dimensions of the device, a very high light emission uniformity can be achieved. Consequently, DDCT LEDs based on GaAs, AlGaAs and GaInP could even facilitate the realization of electroluminescent cooling for practical applications, that may require more efficient charge transport methods.

Zn diffusion into n-GaAs and GaAs/AlGaAs DHJ substrates was successfully demonstrated by using thin SOG coated Zn-films as diffusion sources, and functional light emitting p-n diodes were fabricated on both n-type GaAs and n-type GaAs/AlGaAs DHJ substrates. The IV characteristics of these LEDs showed several non-idealities, but nevertheless the results clearly indicated that Zn diffusion from evaporated zinc thin films could be a viable option for fabricating the suggested DDCT structure. The realization of the novel DDCT LED design still requires further studies, so that the surface damages related to the presence of Zn film can be removed or reduced to an acceptable level. Preliminary diffusion tests performed in a protective N_2 atmosphere gave promising results for enhancing the surface quality. However, this option still requires further studies since the sample surfaces could not be cleaned due to some unexpected chemical reactions during the diffusion annealing.

Despite the very promising results both in terms of simulations and experiments, this work has only scratched the surface upon realizing and characterizing DDCT structures in GaAs based devices. The simulations in this work mainly focused on studying the limiting behaviour of the devices using literature-based material parameters that, apart from the SRH recombination coefficient, were not calibrated according to our experimental measurements. Additionally, the simulations focused mainly on simplified device structures with a simple and symmetric device geometries that are relatively straightforward to fabricate using optical lithography. To fully optimize the devices, relaxing the requirement of symmetry to account for the asymmetric mobility of electrons and holes could lead to better light emission uniformity and capacity for larger current densities. Improved and more detailed device models accounting for e.g. optical transport and localization of the diffusion damage could also reveal interesting optimization possibilities for the devices, if the damage can be contained to regions outside the AR and if photon assisted carrier diffusion and photon recycling effects can extend the effective diffusion lengths of the carriers.

For the experimental work, several topics need further investigations, starting from more detailed investigations of the reproducibility and consistency of the diffusion doping process itself and extending all the way to demonstrating complete laterally doped large area LEDs with an optimized finger structure. In the current work,

selective-area diffusion was not included in the scope of the experimental studies, due to the long time that was required to master the doping process. However, the developed doping technique should be easily modified to allow selective-area doping, which would enable the fabrication of the lateral heterojunctions. With successful fabrication of the simulated devices and removal of the substrate, unique devices for optoelectronic applications could be realized. These include thin film LEDs and solar cells where the extraction or absorption of light is significantly enhanced e.g. by implementing surface plasmon structures or other engineered nanostructures on the device surfaces.

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